

25 W X-band GaN on Si MMIC

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Abstract

The first GaN on Si monolithic microwave integrated circuit (MMIC) has been demonstrated. The 2-stage X-band high power amplifier has a 2.5 mm input stage and an 11.4 mm output stage and its die size is 3 mm x 4.5 mm. At 10 GHz and 30 V drain bias, this MMIC achieved a pulsed output power of 25 W with 15 dB gain and 21% power-added efficiency. It produced 20 W of output power over the 8 to 10.5 GHz band when biased at 24 V. The GaN on Si MMIC was fabricated on TriQuint's 4 inch GaAs manufacturing line and used an existing GaAs design.

INTRODUCTION

Gallium nitride (GaN) grown on silicon (Si) substrates is a very promising technology for microwave applications. It combines the low cost and ease of manufacturing associated with large diameter Si substrates and the demonstrated high power density and high efficiency offered by AlGaIn/GaN devices. Although GaN on SiC substrates potentially offers higher frequency performance (e.g., \geq Ka-band) and better thermal dissipation, SiC is prohibitively expensive and available mostly in 2 and 3 inch diameters that are incompatible with existing commercial GaAs fabs. There is also evidence that GaN on Si devices are more reliable than GaN on SiC [1], perhaps due to nonuniformity or poor quality of the SiC substrate relative to Si. Since 80-90% of the RF market is at X-band or below, the low cost and larger diameter of GaN on Si may lead to insertion in more applications. Most work on GaN on Si to date has targeted commercial applications such as cellular base station amplifiers near 2 GHz [2] with power output densities (Pout) up to 12 W/mm [3].

GaN on Si can also be used to build low cost, high power monolithic microwave integrated circuits (MMICs) at higher frequencies for military, communication or other applications. The first GaN on Si MMIC has been demonstrated by taking a MMIC that was designed for GaAs pHEMT and building it on a GaN on Si wafer. The 100 mm GaN on Si wafers were processed on the TriQuint Texas GaAs manufacturing fab. The resulting X-band GaN on Si MMIC had a similar frequency response to the GaAs MMIC but could be operated at much higher drain biases and delivered higher output power levels. With 24 V of drain bias, 20 W of output power was obtained over the 8 to 10.5

GHz frequency band compared to the nominal 8 W at 9 V that the part delivers on GaAs pHEMT material. This encouraging result indicates the great potential that GaN on Si has for both improving the performance and reducing the cost of MMICs.

PROCESS

The GaN on Si (111) wafers were grown by metalorganic chemical vapor deposition at Nitronex. Nitronex's growth process allows high quality GaN epilayers to be grown on Si substrates by controlling thermal expansion and lattice mismatch-induced stresses [4]. The material described in this study consisted of a 600 nm AlN nucleation layer, a compositionally graded AlGaIn transition layer, a \sim 800 nm unintentionally doped GaN buffer layer and a 300 Å AlGaIn device layer with Al concentration of 20%. Typical sheet carrier concentrations of $6\text{-}7 \times 10^{12} \text{ cm}^{-2}$ and mobilities near $1300 \text{ cm}^2/\text{Vs}$ were measured by Hall effect.

Most GaN development at TriQuint has been done on 2 and 3 inch SiC substrates which are incompatible with the main 4 inch GaAs fab. Thus a separate research fab and equipment is needed to process GaN on SiC wafers. The 4 inch GaN on Si substrates allow production equipment and operators to be used which is inherently less costly and more efficient. There are still GaN specific processing steps that are needed, but they are done on standard equipment.

Standard processing was done in the TriQuint GaAs fab except as noted below. GaN specific processing steps were used in the isolation, ohmic, gate and backside routes. Mesa etching was used for isolation. Inactive regions were defined and RIE etched in a chlorine based chemistry. With 80 V applied across a 10 μm isolated gap, less than 10 nA/mm of current was observed on all wafers.

The ohmic metal was Ti/Al based and the RTA alloy was done at 850 °C. Ohmic deposition on wafers 1 and 3 and RTA alloy of wafer 1 was performed at Nitronex. A TriQuint RTA that aimed to copy the Nitronex process was used on wafers 2 and 3. Resulting contact and sheet resistances are given in Table 1 and averaged 0.6 ohm-mm and 720 ohms/square, respectively. This matches closely with wafers processed in the Nitronex fab on similar material. No gate recess etching was performed on these wafers. A dielectrically defined field plate gate was patterned and Pt/Au

TABLE 1
OHMIC PROCESS SPLIT BETWEEN TRIQUINT (TQ) AND NITRONEX (NTRX) FABS GAVE SIMILAR CONTACT (Rc) AND SHEET (Rsh) RESISTANCE.

Wafer	Ohmic dep at	RTA at	Rc ohm-mm	Rsh ohm/sq
1	NTRX	NTRX	0.64	705
2	TQ	TQ	0.65	726
3	NTRX	TQ	0.51	717
AVG			0.60	716

was evaporated for the gate metal. The optical process defined a 0.30 μm gate length “T-shaped” gate.

The rest of the frontside process used TriQuint’s standard flow for interconnect metal, capacitors and airbridges. The backside grinding to 4 mils and etching via holes through the Si substrate was done by Nitronex using standard Si process technology. An ICP etch of the GaN epitaxial layers was done at TriQuint to complete the via hole etch. This was followed by backside metallization and die separation by sawing.

DC RESULTS AND YIELD

Post gate metal DC results are summarized in Table 2. Wafer to wafer variations were small and standard deviations were near 4 %. Average $I_{D,max}$ of 570 mA/mm was measured at $V_g = 2$ V and $V_d = 10$ V and is about 10% lower than similar material processed at Nitronex. More careful GaN optimization of certain GaAs optimized processing steps such as asher and resist cleanup steps may improve $I_{D,max}$. Two-terminal breakdown voltage (defined at 1 mA/mm) was near 90 V.

Full wafer DC automated probing of the 451 MMICs per wafer showed good yields for 2 of the 3 wafers and standard deviations near 5 %. Several parameters were measured on both the input and output transistors of the MMIC which measure 2.5 mm and 11.4 mm, respectively. DC yields for wafers 1, 2 and 3 were 72, 5 and 85%, respectively. Wafer 2 was misprocessed during the liftoff of its first metal leaving most MMICs with unconnected gates and very low yield. Most of the yield loss on wafers 1 and 3 was due to pinchoff failures, possibly due to lifting gates or contamination under

TABLE 2
POST GATE DC DATA OF THE 3 WAFERS.

Wafer	Gm,max (mS/mm)	Idss (mA/mm)	Idmax (mA/mm)	Idleak (nA/mm)	Vp (V)	BVdg (V)
1	189	379	572	1040	-2.65	99
2	173	343	555	380	-2.54	85
3	192	374	582	2730	-2.52	78
avg	185	365	570	1380	-2.57	87

the gate. The pinchoff voltage of wafers 1 and 3 was -2.74 and -2.53 V, respectively, and standard deviations were 5.5% for both. Wafer maps show a slight increase in $I_{D,max}$ moving radially outward from the center, most likely attributable to a slight increase in Al % and growth temperature near the wafer edge, but the standard deviation was still only 5.4%.

RF SMALL SIGNAL AND LOAD PULL RESULTS

On wafer small signal measurements were collected on $4 \times 75 \mu\text{m}$ devices from 1 to 40 GHz using an HP8510C network analyzer. H21 and MSG/MAG were calculated and values for the cutoff frequency, f_t , and maximum frequency of oscillation, f_{MAX} , were extracted. Data were fit using an equivalent circuit model. Measured and modeled data for H21 and MSG/MAG are shown in Figure 1 from which an f_t of 22 GHz and an f_{MAX} of 74 GHz were extracted for wafer 1 at a drain bias of 20 V and 100 mA/mm. Figure 2 shows the decline of f_t with increasing drain voltage but still above X-band even at 40 V.

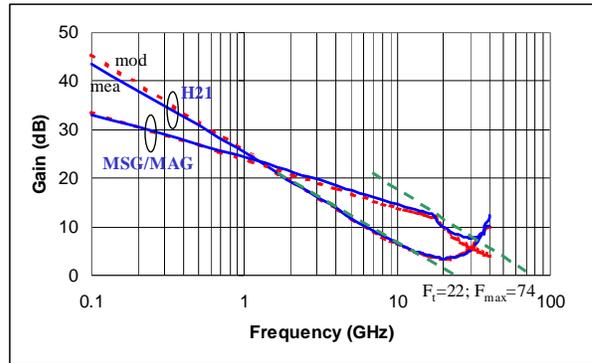


Figure 1. Measured and modeled H21 and MSG/MAG vs. frequency for wafer 1 showing f_t of 22 GHz and f_{max} of 74 GHz when biased at 20 V and 100 mA/mm.

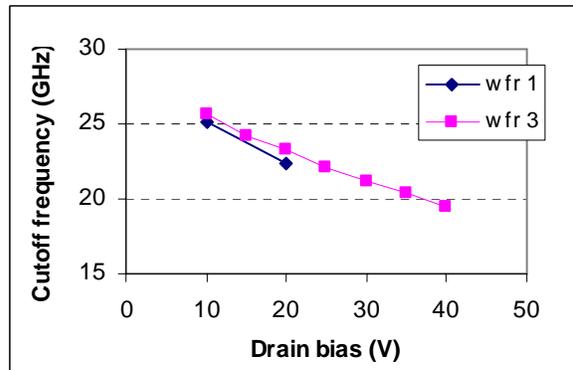


Figure 2. Cutoff frequency, f_t , vs drain bias at $I_d=100$ mA/mm for $4 \times 75 \mu\text{m}$ devices.

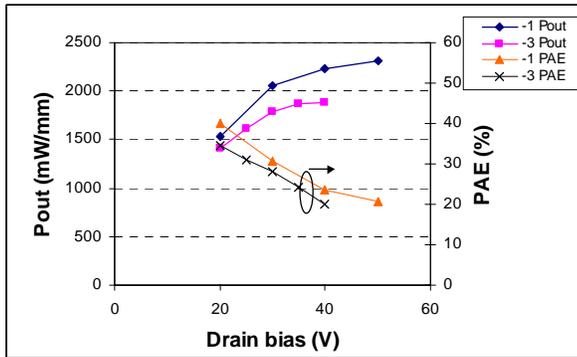


Figure 3. Power output density and PAE vs. drain bias for 4x75 μm devices at 10 GHz.

Load pull data were taken on wafers 1 and 3. On-wafer CW measurements were collected on 4x75 μm devices using Focus Microwave tuners. Load pull at 10 GHz and 40 V drain bias resulted in 2.2 W/mm with 23.5 % PAE and 8.7 dB associated gain on wafer 1. Wafer 3 was slightly less at 1.9 W/mm, 20.1 % PAE and 9.8 dB associated gain for the same conditions. All load pull measurements are given at the peak of PAE and tuned for maximum power. Figure 3 shows Pout and PAE vs drain bias at 10 GHz. The associated gain for the results in Figure 3 are all close to 10 dB. A lot processed at TriQuint with more recent material from Nitronex gave 5.4 W/mm, 30.1 % PAE and 10.1 dB of gain at 10 GHz. In addition, Nitronex has obtained 12 W/mm at 2.1 GHz on small periphery discrete devices using the new material structure [3].

In order to investigate the limitation of this technology on Si substrates, we compared the loss of transmission lines on GaN on Si wafers to other substrates. Microstrip lines of length 2.9 mm were fabricated. The loss on GaAs was 0.03 dB/mm, and the loss on GaN on Si was only slightly higher at 0.08 dB/mm at 10 GHz. These results show that the microstrip loss will not be a limitation for this technology at X-band. Table 3 summarizes the line loss for 2, 10 and 20 GHz for the 2.9 mm microstrip lines built on 4 different substrates: GaAs, GaN on SiC, Si and GaN on Si.

TABLE 3
LINE LOSS IN dB/mm FOR A 2.9 mm MICROSTRIP LINE FABRICATED ON 4 DIFFERENT SUBSTRATES.

Freq. GHz	GaAs 4 mil	GaN/SiC 4 mil	Si 5 mil	GaN/Si 4 mil
2	0.005	0.005	0.025	0.065
10	0.025	0.020	0.050	0.080
20	0.040	0.035	0.080	0.140

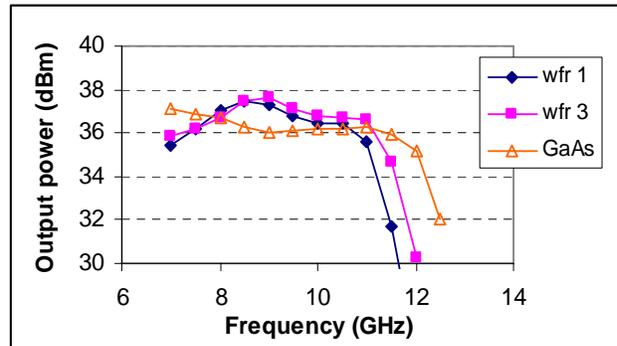


Figure 4. On wafer RF probe of the MMIC for 2 GaN on Si wafers (at 12 V) and a standard GaAs wafer (at 7 V). Data represent the 50th percentile.

RF MMIC TESTING

In MMIC testing at X-band, full wafer RF probe demonstrated both high yield and increased output power at elevated drain bias. RF yield was 78 and 85% for wafers 1 and 3, respectively. The drain bias for on-wafer testing was limited to 12 V which produced 5.5 W at 9 GHz compared to 4.0 W at 7 V for the GaAs version. Data representing the 50th percentile are shown in Figure 4 for wafers 1 and 3 and a standard GaAs wafer. The frequency response of this design on GaN on Si wafers was surprisingly similar to that of the standard GaAs pHEMT product (TriQuint part TGA9083).

Several GaN on Si MMICs from wafer 1 were assembled in fixtures for pulsed power testing at higher drain biases. Die size is 3mm x 4.5 mm. A 50 microsecond pulse was used with a 10% duty cycle. Figure 5 shows the output power of the MMIC at 10 GHz with 30 dBm input power and drain voltage varying from 12 to 30 V. At 30 V drain bias, 25.4 W output power, 21% PAE and 14.8 dB gain were measured.

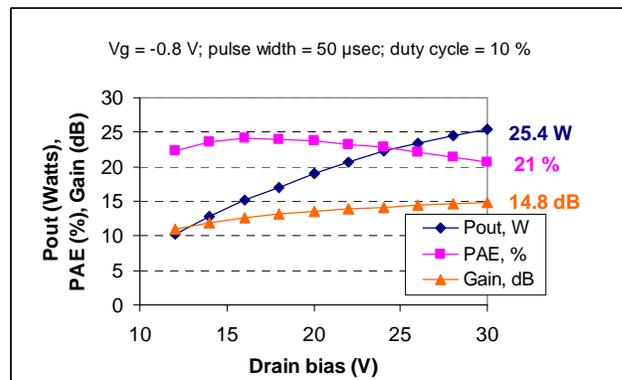


Figure 5. Pulsed power output, PAE and gain of the X-band MMIC at 10 GHz vs. drain bias. Peak power is 25.4 W at 30 V for the X-band MMIC.

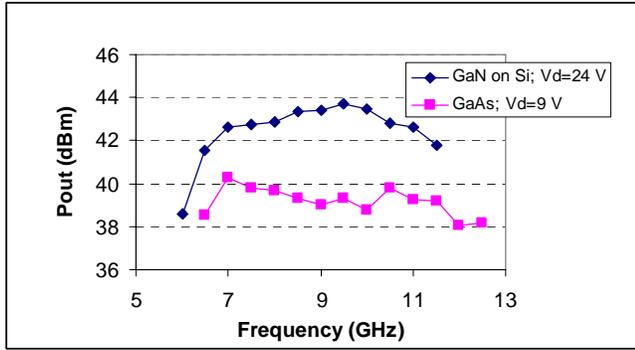


Figure 6. Frequency response of fixtured X-band MMICs showing GaN on Si (wafer 1) biased at 24 V and a GaAs pHEMT wafer biased at 9 V.

This represents about 6 dB of compression. Backing off 3 dB from that point gives 20.6 W output power, 27% PAE and 17.9 dB of gain. Figure 6 shows the frequency response of the fixtured device with Vd of 24 V and 3 dB of compression. Twenty watts is achieved across a frequency band from 8 to 10.5 GHz. The fixtured performance of this part on GaAs pHEMT at 9 V drain bias is also plotted. A design specifically made for GaN on Si should provide even better performance, especially using the latest generation of Nitronex material and an optimized process.

CONCLUSION

A 25 W X-band high power amplifier has been realized using GaN on Si substrates. This opens up new MMIC applications for this promising technology. Combining the high power output density and high voltage capability of GaN with Si substrates provides a low cost alternative to GaN on SiC for next generation HPA requirements. Using Si substrates also gives compatibility with existing GaAs fabs and equipment. Various applications in the commercial, communication and military segments are envisioned.

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ACRONYMS

- AlGaIn: Aluminum Gallium Nitride
- GaAs: Gallium Arsenide
- GaN: Gallium Nitride
- H21: Forward Current Gain
- HFET: Heterostructure Field Effect Transistor
- HPA: High Power Amplifier
- ICP: Inductively Coupled Plasma
- MAG: Maximum Available Gain
- MMIC: Monolithic Microwave Integrated Circuit
- MSG: Maximum Stable Gain
- PAE: Power Added Efficiency
- pHEMT: Pseudomorphic High Electron Mobility Transistor
- Pout: Power Output Density
- RTA: Rapid Thermal Anneal
- Si: Silicon
- SiC: Silicon Carbide