Performance and Fabrication of GaN/AlGaN Power MMIC at 10 GHz

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ABSTRACT

High performance and fabrication of a coplanar 2 stage power amplifier based on a GaN/AlGaN HEMT technology on 2-inch SiC substrate has been realized. At 10 GHz the coplanar MMIC delivers a maximum output power of 13.4 W, measured on wafer in pulsed mode, a linear gain of 20 dB and a maximum PAE of 25 % at a V_{DS} bias of 35 V and compression level of 5 dB. The yield of the MMICs across 2-inch wafer is 65 %.

I. INTRODUCTION

Gallium Nitride (GaN) HEMTs are the focus of intense research and development due to their potential for the realization of MMIC power amplifiers (PAs) with high gain and record levels of power delivery to be used in commercial and military systems [1]. The outstanding power performance of these devices is a result of the high electric breakdown field in wide band gap nitride semiconductors, high electron saturation velocity in GaN, and good thermal conductivity of SiC substrates. Much of the work in GaN HEMT development has been concentrated on performance demonstration on single or large devices; there are few reports on GaN HEMT based power amplifiers reproducing the excellent results shown for the HEMT devices [2,3]. We report on the fabrication and performance of GaN/AlGaN coplanar 2 stage power amplifier on 2-inch SiC substrate. The MMICs exhibit a maximum output power of 13.4 W, measured on wafer at 10 GHz in pulsed mode at a V_{DS} bias of 35 V. The yield of the MMIC across 2-inch substrates was about 65 %. Devices with gate periphery of 1 mm measured at 10 GHz CW yielded maximum power densities of 5.2 W/mm and a maximum PAE of 31 % at V_{DS} = 35 V.

II. DEVICE AND PROCESSING

The AlGaN/GaN heterostructure is grown by metal organic vapor phase epitaxy on s.i. SiC substrate and consisted of 250 nm AlGaN nucleation layer, a 2.4 µm GaN buffer, an undoped AlGaN barrier layer with 30 % of Al and GaN cap layer.

An eight-mask-level MMIC process is used to fabricate the devices and the circuits. Device fabrication consisted of mesa definition using a Cl_2-based electron-cyclotron resonance (ECR) etching tool. Ohmic contact was accomplished by the use of a Ti/Al/Ni/Au metal stack annealed in N_2. The 0.3 µm T-gates employing Ni/Au Schottky contact are formed using direct e-beam writing. The passivation was done using an ECR silicon nitride. Two levels of interconnect metal including air bridges, 50 Ω/sq NiCr resistors and MIM capacitors with breakdown voltages over 200 V are used to complete the fabrication of the MMIC.
Transistors with gate widths of 2x50 µm and 8x125 µm reached maximum drain currents of 1.35 A/mm and 0.93 A/mm at V_{DS} = 7 V, respectively and average values for the maximum transconductance of 285 mS/mm and 245 mS/mm, respectively. The 100 µm and 1 mm gate width device showed an f_T -values of 43 GHz and 40 GHz, respectively and f_{max} - values of 100 GHz and 65 GHz, respectively. The standard deviation across 2- inch wafer of the DC and RF parameters is excellent and the yield is higher than 85 % as shown in Fig 1.

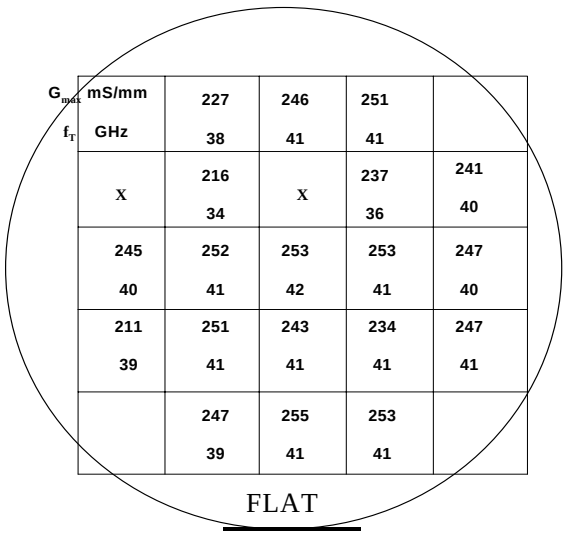

Fig.1 : Uniformity and yield across a 2-inch SiC substrate of the maximum transconductance and f_T for 8x125 µm gate width GaN HEMTs at drain bias of 7 V.

Pulsed I-V measurements of an 8x125 µm device were taken on the ACCENT DIVA dynamic I-V analyzer, where both the gate and drain of a HEMT are pulsed on top of the DC bias conditions. Fig. 2 shows the DC and pulsed I-V characteristics of the passivated device on SiC substrate. At pulse width of 1 µs, low dispersion was observed and the drain current in pulse operation is not severely limited by surface traps.

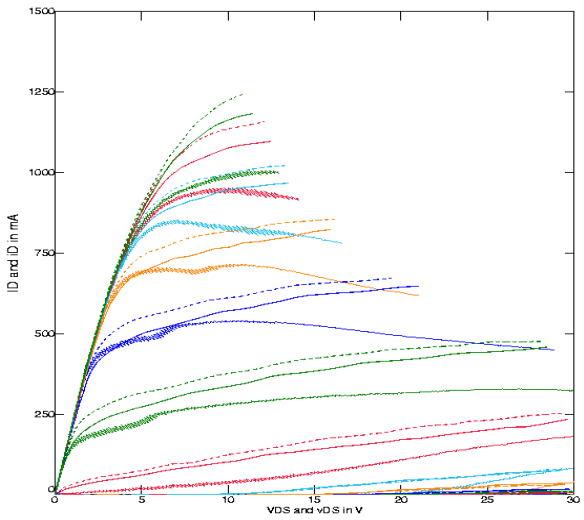

Fig.2 : DC (thick solid line) and pulsed I-V curves taken at V_{DS}=0 V and V_{GS}= 0 V (dashed line) , V_{DS}=30 V and V_{GS}=-7 V (thin solid line), pulse width 1 µs, pulse repetition 1 KHz.

We performed DC lifetime tests to reveal degradation mechanisms due to the applied bias and current flow. FET's with 50 µm gate width, taken across 2-inch substrate, were stressed in air at an ambient temperature of 200° C under power dissipation of 5 W/mm (V_{DS}= 20 V and I_{DS}= 250 mA/mm). Fig. 3 shows the relative changes in I_{DS} for the FET's. We have a rapid drop in the current during the first hours of test, then a stabilization as a function of time. The failure criterion is defined as 20 % degradation in I_{DS}. Metal-insulator-metal (MIM) capacitor is a key passive component in the GaN-based power amplifier MMIC technology. We have developed a silicon nitride film using a PECVD method, using SiH_4, NH_3 and N_2 gaseous species at 240° C. The dielectric film has a capacitance density of 12 pF/mm^2 and can at least tolerate voltages higher than 200 V with absolute current in the order of few tens of nanoamperes. Fig. 4 shows I-V curves of a 300x400 µm^2 MIM capacitors across 2-inch SiC substrate, we demonstrate a good uniformity and yield across the wafer, this result was reproduced on 10 other SiC substrates.

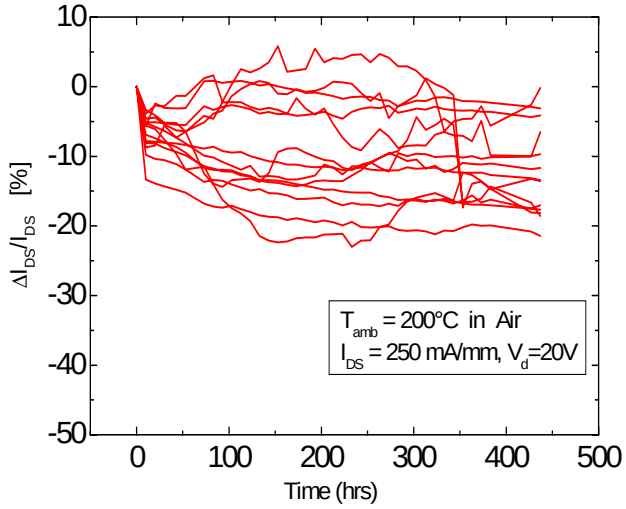

Fig.3 : Relative change in I_{DS} of GaN HEMTs stressed in air ambient at V_{DS} = 20 V, I_{DS} = 250 mA/mm and T_{amb} = 200°C .

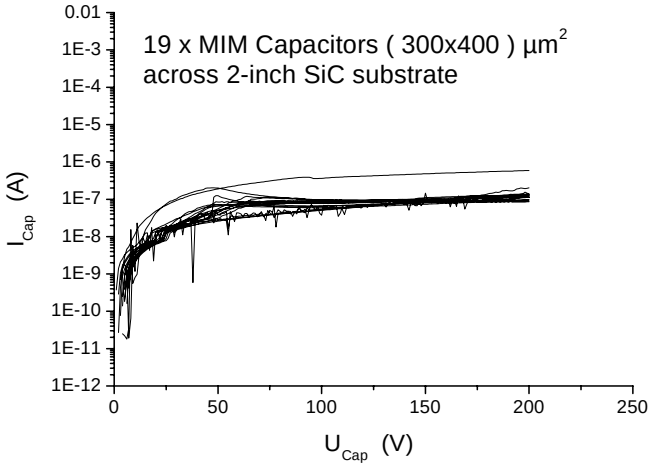

Fig.4 : I-V curve of MIM capacitors on 2-inch SiC with 500 nm PECVD silicon nitride tolerating at least 200 V.

III. X-BAND POWER AMPLIFIER

On-wafer microwave power measurements were performed for a 8x125 µm gate width device at 35 V drain bias. A CW output power density of 5.2 W/mm at 10 GHz was measured with a linear gain of 11 dB and a maximum PAE of 31 %, as shown in Fig. 5. The power measurements were performed across the 2-inch substrate for the 8x125 µm transistors. We demonstrate a device yield higher than 80 % with an average maximum power density of 5 W/mm.

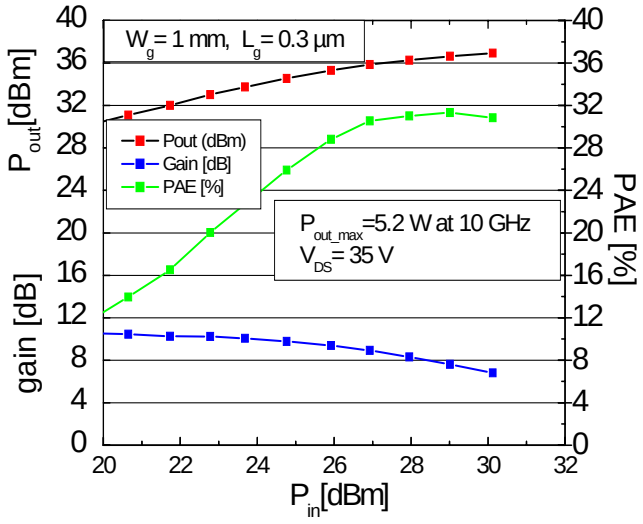

Fig.5 : 10 GHz CW load-pull performance of (8x125) µm AlGaN/GaN HEMT on SiC substrate at V_{DS}= 35 V.

A two-stage high power amplifier, with chip size of 4.5mmx3mm, was designed with a 2-mm input driving a 4-mm output, the power amplifier was tested on wafer. Scattering parameters of the MMIC were taken at V_{DS}= 25V and I_{DS} = 175 mA/mm and are shown in Fig. 6. The 0.3 µm gate length power MMIC shows 17 dB of measured gain at 10 GHz in CW mode.

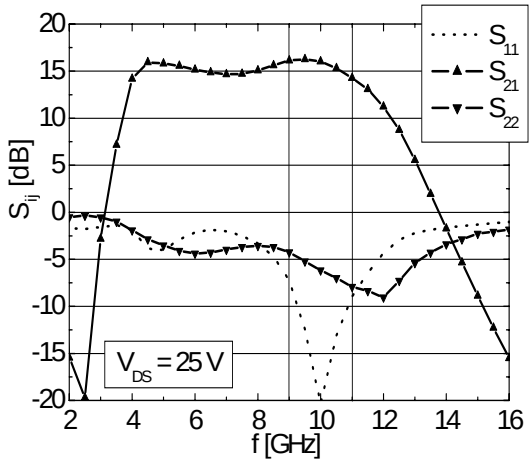

Fig.6 : Measured scattering parameters of the power amplifier under conditions of V_{DS}= 25 V and I_{DS}=175 mA/mm.

Fig. 7 shows a 10 GHz pulsed power sweep of a GaN power amplifier tuned in class AB operation, at V_{DS}=35 V, 100 µs pulse width, pulse repetition 1 kHz and 10 % duty cycle. The MMIC exhibits a peak power level of 13.4 W with an associated gain of 15 dB, a linear gain of 20 dB. The PAE is estimated to be 25 %. The yield across the 2" substrate is about 65%. A better thermal management and a new design can improve the power performances.

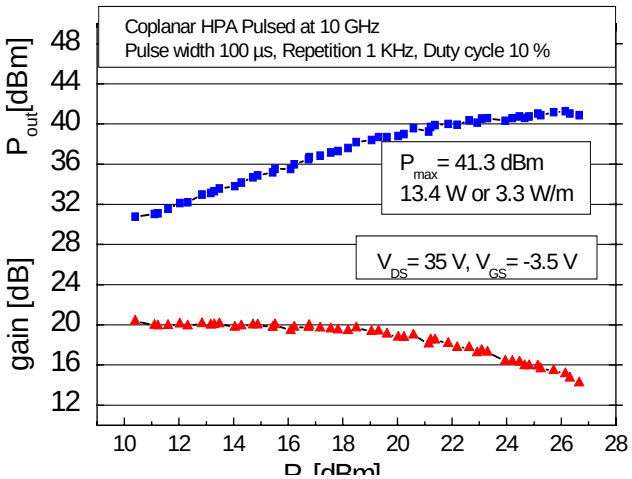

Fig.7 : Pulsed power performance of power amplifier at 10 GHz with maximum P_{OUT} of 41.3 dBm at 35 V drain bias.

IV. CONCLUSION

An AlGaN/GaN based HEMT coplanar technology used for the fabrication of a power MMIC on 2-inch wafer is presented. At 35 V in pulse mode, the 2 stage power MMIC delivers 13.4 W maximum power with 25 % maximum PAE at 10 GHz, with a yield of 65 %. The 1 mm gate width device exhibits a maximum power density of 5.2 W/mm CW at 10 GHz with a yield of 85 %.

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