A Novel Approach For Hermetic Wafer Scale MEMS RF and GaAs Packaging

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Abstract

Technical advances in RF and GaAs devices have generally outpaced those in device packaging. This disparity has created a situation where packaging technology can become a limiter to device performance. A process strategy is presented here for massively parallel creation of hermetic wafer scale packaging for RF devices.

Introduction

Device packaging is an aspect of compound semiconductor and optical device manufacturing technologies which is frequently overlooked or even ignored.

However, packaging selection not only affects total system price and COO (cost of ownership) it can and often does impact ultimate device performance. Wafer scale packaging is one technological approach which maximizes the footprint available to the die or device while minimizing the overall package or device size. The die or substrate itself becomes an integral part of the package rather than requiring the die or device to be encapsulated within a secondary level package.

System reliability is another concern which in the case of MEMS, photonics and optoelectronic devices typically manifests itself as requirements for system hermeticity environmental mechanical integrity and zero outgassing within the package during assembly or use. The use of Au/Sn eutectic solder is a time tested means of reliably accomplishing hermetic device sealing, but has been historically limited to the use of performs inappropriate for wafer scale use, or as a solder paste which poses a high risk for device contamination and imposes a requirement for post-cleaning during processing.

PVD processes alone can sidestep most of these limitations, but typically require many hours of processing time in capital equipment.

We have endeavored to advance manufacturing technology for MEMS and photonics devices by creating a wafer scale packaging technology which permits devices to be packaged in a massively parallel fashion, following device testing but prior to wafer singulation. Wafers or substrates are processed individually, minimizing the yield loss risk to the process owner compared to batch processing systems.

This processing technology incorporates the best aspects of vacuum processing and electrochemical technology, while minimizing the drawbacks of both. Fine features for device interconnect and sealing are firs patterned by vacuum deposition. A wide variety of metallurgies are available which can be tailored to the particular device and application. The bulk package or interconnect metallurgy is then electrochemically deposited onto the PVD base metalization in a massively parallel fashion. Not only Au/Sn, but Cu, Sn In or any of the known solder or braze alloy composition stoichiometries can be deposited at resolutions associated with vacuum processing but at process speeds which are orders of magnitude more rapid.

Process experiments carried out with patterned Au/Sn solder deposits on Si and glass wafers have shown that a high degree of dimensional and compositional control commensurate with a high reliability manufacturing process can be maintained.

Background

Gold-tin soldering (80%Au:20%Sn) has historically been used in the microelectronics industry for lid sealing and die attach applications. are used to bond large metal components together. Package lids, heat sinks, and die are joined by inserting a Au-Sn preform between the surfaces to be sealed, pressing them together and applying heat.

Where the use of preforms is impractical or impossible, the AuSn alloy can be created using electroplating techniques. Alternating layers of pure gold and tin are selectively deposited to effectively create a patterned Au-Sn preform *in situ.* It is also possible to deposit an AuSn metal stack using PVD evaporation or sputtering, but vacuum processes are generally limited to depositing extremely thin AuSn coatings, due to the slow deposition rate and the correspondingly long processing times required. Functional evaporated Au-Sn layers as thick as 5000 Å have been regularly successfully deposited via PVD, but greater seal thicknesses are only occasionally seen.

For those circumstances where it is not possible to fabricate a stamped preform that will meet assembly requirements, an *in situ* preform can be created using a combination of photolithography and electroplating. In this process, a phototool is prepared replicating the pattern shape and line width of the desired solder bond layout. The backside metallization of one the component surfaces is coated with either dry or spin-on photoresist and then patterned and developed using standard lithographic protocols. The patterned wafer surfaces are then plated sequentially with gold and tin to create an 80Au-20Sn solder alloy pattern. Following plating the photoresist is stripped from the wafers; the parts are cleaned, aligned and reflowed to create the hermetic joint. AuSn alloy reflow takes place in a precisely controlled low oxygen- neutral or reducing soldering atmosphere. AuSn reflow does not require the use of flux, which eliminates any requirement for post-reflow cleaning.

AuSn offers several advantages when creating hermetic solder joints and packaging elements at wafer scale. Among them are a high liquidus onset and the ability to create a hermetic joint between metalized surfaces without recourse to flux. AuSn also imparts superior thermal and electrical properties to the device packaging when compared to other solders and brazes. AuSn also possesses a low intermetallic growth rate when used in conjunction with Ni, Ta, Ti, Pd or Pt PVD base metalizations.

Metallurgy of AuSn

The AuSn phase diagram is a eutectic binary-phase diagram with two eutectic melting points, one at 80% Au (278°C) and one at 10% Au (217 °C). [Fig. 1]
It is the 80% gold alloy that is used for fluxless soldering. The 80:20 AuSn eutectic consists of AuSn and Au_5Sn intermetallic phases. The eutectic alloy consists of 64.3% Au_5Sn and 35.7% AuSn by mass. No free tin exists in the true eutectic. Tin is found as the mixture of the two intermetallic compounds. Note that this zone of the phase diagram is defined by very steep liquidus lines on both sides of the eutectic melting point, indicating that enriching the composition by one percent of gold leads to an approximate 30 °C increase in melting temperature. For this reason, the creation of AuSn solder forms requires accurate control of solder composition and bonding temperature. The other eutectic alloy, 10:90 AuSn, will not produce reliable solder joints due to the formation of a brittle $AuSn_4$ intermetallic within the solder joint.

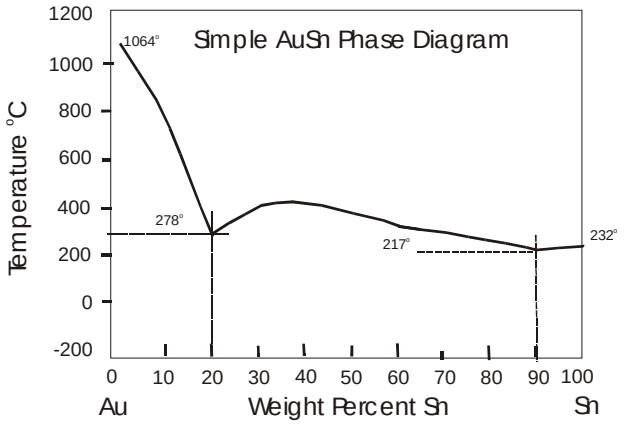

Fig.1- Au-Sn phase diagram

Test Article Construction and Evaluation

A wafer test article (as shown below) was designed and constructed to evaluate the functional properties of the electrodeposited AuSn in a wafer scale packaging application. The test wafer is 150 mm in diameter with a 68 test packages/die which are 15 mm x 12 mm. The die seal surface trace width is 80 µm with a pitch (separation) between die of 50 µm. The basis metallurgy was applied using standard PVD methods and consists of 250 Å Ta and 750 Å Cu with a top layer of immersion Au of approximately 100-200 Å. Thick film dry photoresist (TOK 50120) was applied and photolithographically patterned to develop the desired metallurgy dimensions. The nominal process target for the electrodeposited AuSn metallurgy thickness was 20 µm. Following deposition the test die thicknesses were

characterized using a Dektak 6M profilometer. Metallurgy reflow was accomplished in an N_2 atmosphere with a pO_2 of less than 50 ppm at a peak temperature of 320C.

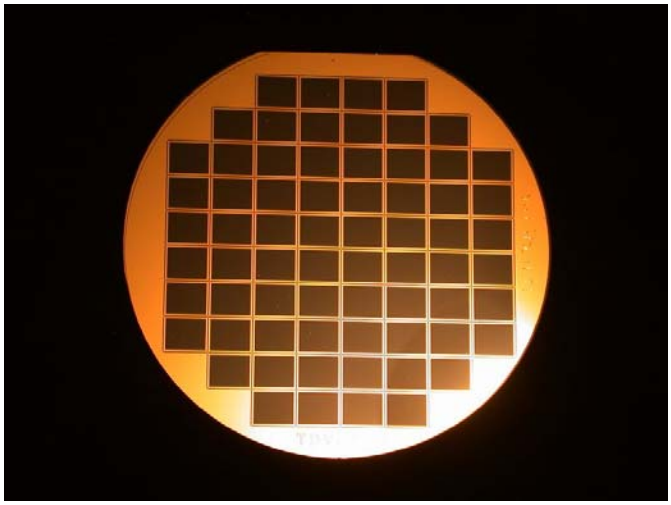

Fig.2- Test wafer

Results

Deposit thickness was characterized on all of the test wafer traces. For N=168, the mean deposit thickness was found to be 20.1 μm with a standard deviation of 0.49 μm.

Following reflow, metallurgy bond strength was characterized using die shear value measurements as per MIL-STD-883E Method 2019.7 . For N=79, the mean die shear force was found to be 0.13 kg, with a standard deviation of 0.02 kg.

Hermeticity of the reflowed joints was characterized as per MIL-STD-883D using the He fine leak measurement technique. The mean He leak rate was found to be $< 10^{-7}$ cc He/s.

Conclusions

Creation of hermetic wafer scale RF MEMS and MOEMS packaging by massively parallel electrochemical deposition has been shown to be a commercially viable manufacturing approach. AuSn eutectic solder is an ideal material for the creation of robust hermetic metallurgical bonds without the use of flux, particularly important for photonics and MEMS applications where the entrapment of flux residues would render the device inoperable.

A wide variety of other metals can also be deposited using single wafer electrodeposition to create wafer package bonds and wafer features such as Cu vias/posts and I/O interconnect.

The next phase of this development process will be to characterize the functional attributes of the wafer scale packages following repeated thermal cycling with and without application of voltage bias.

References

[1] C.H. Lee, Y. M. Wong, J. Appl.Phys. 72 (8), 3808, October 1992

[2] SST International, Downey, CA

[3] AIM Specialty Materials, Cranston, RI

[4] Surfect Technologies, Albuquerque, NM