

Recent Progress of Highly Reliable GaN-HEMT for Mass Production

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Abstract

In this paper, we describe the recent progress of highly reliable GaN high electron mobility transistors (HEMTs) for mass production. We introduce reliability data of recent GaN-HEMT. There are three phases to understand the reliability. Yield issues are discussed considering surface hexagonal pits. Cost is most important issues after reliability is confirmed. Highly uniform low cost GaN-HEMT using a conductive 3-inch SiC substrate will be reported. In addition, future base station requires extremely high efficiency, requiring GaN-HEMT to be used at saturation region. An over 100 W GaN-HEMT using metal-insulator-semiconductor (MIS) gate is demonstrated to suppress the forward gate leakage current at saturation region.

INTRODUCTION

Wireless mobile networks are expected to move up to 4G technologies from 2010. As transmission speeds will be over 100 Mbps, higher speeds and increased output power will be required, leading to increased power consumption of transmission amplifiers and thereby resulting in base stations that require significantly higher power and more physical space. Given this, there is a need for the development of wireless mobile base stations for which less space is required that are easily implemented and with low operation costs.

To enable lower power consumption, high efficiency GaN-HEMT amplifiers are currently being developed for 3G networks. GaN-HEMT has high breakdown voltage with high cutoff frequency compared with other material based devices (Fig. 1). We have already obtained 250 W GaN-HEMT push-pull amplifiers with high efficiency under W-CDMA signals [1,2]. It is obvious that the advantage of GaN-HEMT is "high efficiency" due to high breakdown voltage.

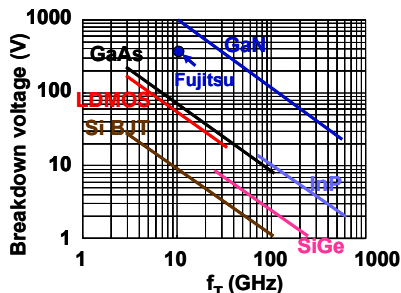


Fig. 1 Johnson's figure of merit.

Reliability is the first priority issue to be confirmed for mass production. To enter the market, reliability should be proven. In this paper, we categorize the degradation phenomena. Yield and reproducibility are also introduced.

Distortion characteristics such as the memory effect are also important issues for wireless base station application. Small memory effect was confirmed using a SiC substrate.

Cost should be considered to obtain high share in the market. Usually, these GaN power HEMTs are fabricated on semi-insulating (S.I.) SiC substrates, which are commercially available but prohibitively expensive for now. One candidate to overthrow the conventional Si-LDMOS is an n-type doped SiC substrate that has high thermal conductivity. In this paper, highly uniform GaN-HEMT with high gain on a 3-inch conductive SiC substrate is introduced without any changing thermal memory effect, which might be significant when Si or sapphire is used [3-5].

Next generation networks will necessitate much higher power efficiency to dramatically reduce the increased power consumption, requiring GaN-HEMT to be used at saturation region. However, forward gate leakage current increases as input power increases, creating problems in terms of reliability and amplification characteristics. To improve the forward gate leakage current, we developed GaN-MIS-HEMT which can be operated at 60 V with 110 W [6].

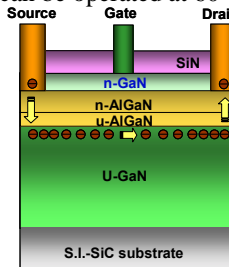


Fig. 2 Schematic cross sectional view of AlGaIn/GaN HEMT with surface-charge-controlled n-GaN-cap structure.

EXPERIMENTAL

To suppress instability related to large-signal current collapse and gm dispersion, we used an n-type doped GaN cap layer in the AlGaIn/GaN HEMTs and controlled polarization-induced surface charges (Fig. 2). Details of the fabrication method have been described previously [1-6]. Recessed ohmic technology was used to reduce ohmic contact resistance. The current-collapse-free surface-charge-

controlled AlGaIn/GaN HEMT die was mounted on a conventional metal/ceramic package.

RESULTS

1) Reliability [1,2,7]

There are three important categories in reliability. Phase I: Rapid gradual gate degradation was observed within a 10 sec during high temperature deep class-AB DC stress test (Fig. 3). This might be attributed to stability of the interface between the gate electrode and GaN surface.

Phase II: Sudden degradation occurred for around 1-2 hours during high temperature pinched-off DC stress test (Fig. 4). This is quite important phenomenon to obtain high reliability. Both process and epitaxial layer affects this degradation. Figure 5 shows gate leakage current before and after the stress test. Although the degradation happened, gate current only around V_g of 0 V increased at room temperature measurements. At high temperature measurements, gate leakage current increased drastically after sudden degradation. Thus, this degradation might be originated from gate leakage pass appeared at high temperature.

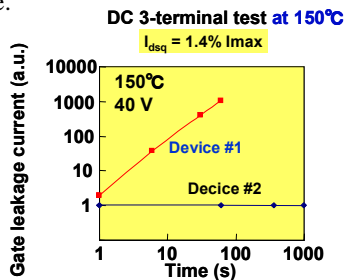


Fig. 3 Phase I: Pout and drain current stability under RF-stress test.

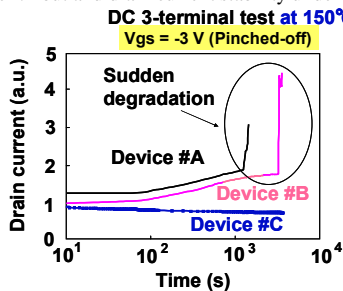


Fig. 4 Phase II: Pout and drain current stability under RF-stress test.

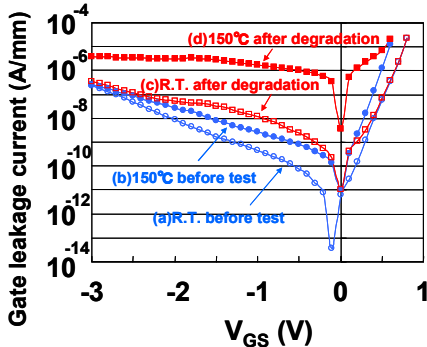


Fig. 5 Gate leakage current of degraded chip in Fig. 4.

Phase III: Gradual degradation less than 0.5 dB of output power was observed for 10 hours during room temperature P3dB-RF stress test. These three phenomena have been observed by many researchers. Both process condition of surface layer and growth condition of a buffer layer are quite important to improve this degradation. This could be suppressed in our structure (Fig. 6). No degradation of I_{ds} , i.e. efficiency, was confirmed, suggesting that reliability of GaN-HEMT becomes to be proven. This improvement was obtained by optimizing pulsed I-V characteristics (Fig. 7).

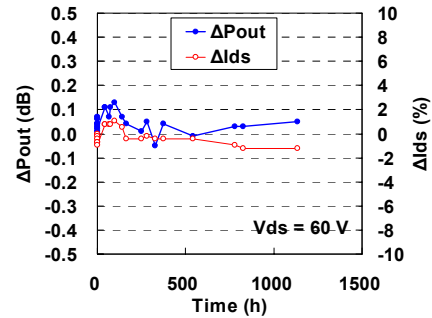


Fig. 6 Phase III: Pout and drain current stability under RF-stress test.

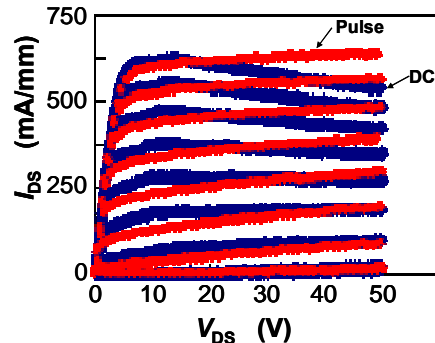


Fig. 7 DC and Pulsed I-V characteristics. Bias point of pulsed measurements was V_{ds} of 50 V and V_{gs} of -2 V. Pulse period and pulse duration are 1 ms and 0.2 μ s, respectively. V_{gs} was varied from -2 to 2 V by 0.5 V step. I_{max} was 600 mA/mm in this case

2) Yield and Reproducibility [7]

Yield is quite important issues to determine the cost. Surface morphology might affect yield of large die. In this study, effect of pits was investigated, because GaN epitaxial layer on SiC substrates includes many types of pits.

Figure 8 shows photograph of a typical hexagonal pit observed on GaN-HEMT epitaxial layer grown by MOVPE. Effect of pits which touched gate electrodes was investigated. Figure 9 shows sub-threshold characteristics of large gate-periphery die. When number of hexagonal pits was increased, pinched-off current increased, resulting in low yield. These increments were too small to detect when a small gate-periphery die such as less than 1 mm was used. Low hexagonal pit density is required to obtain high yield of large gate-periphery die which produces over 100 W.

Figure 10 shows reproducibility of PAE among 60 wafers. On-wafer load-pull measurement was performed

under power-match condition. Gate width is 1 mm. All wafers showed higher PAE over 55%, demonstrating stable growth and processing technology.

3) Memory effect of distortion [7]

Third order intermodulation (IM3) of two tone CW measurement as a function of frequency separation is shown in Fig. 11. Memory effect was quite small between 200 kHz and 5 MHz. This small memory effect is due to high load impedance and good thermal conductivity of SiC. This small memory effect is the advantage of a SiC substrate.

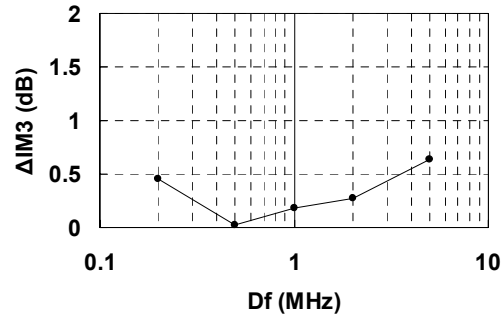


Fig. 11 Memory effect of 50-W GaN-HEMT. IM3 as a function of frequency separation is shown.

Hexagonal pit

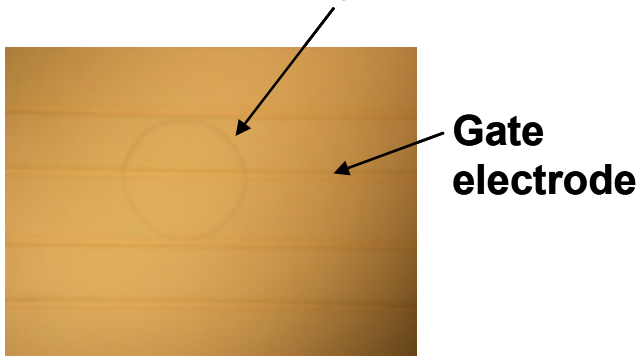


Fig. 8 Photograph of a hexagonal pit on surface which touches gate electrodes of a large gate periphery die.

4) Low cost using a 3-inch conductive SiC substrate [3-5]

To overcome the problem due to the conductive substrate such as parasitic capacitance and isolation leakage, a HVPE-grown 10- μm -thick AlN buffer layer was inserted between n-SiC substrate and MOVPE-grown GaN-HEMT structure. We previously reported a 100 W output power at high drain bias voltage of 60 V using a 2-inch conductive SiC substrate [3].

MOVPE-grown buffer conditions on the oxidized AlN surface were optimized to obtain a smooth surface. Two different AlN layer were compared as shown in Fig. 12. GaN surface morphology by AFM was strongly affected by AlN quality (Fig. 13). Table 1 is the summary of the effect of AlN layer on HEMT performance. Power characteristics were also influenced by the AlN layer.

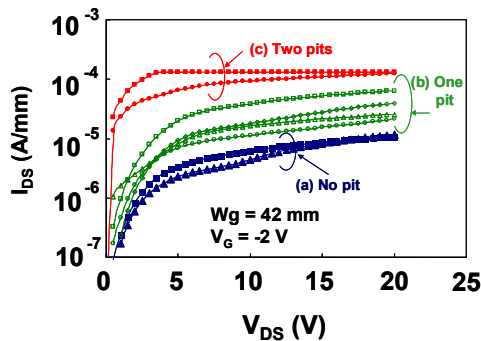


Fig. 9 Effect of hexagonal pits on sub-threshold characteristics.

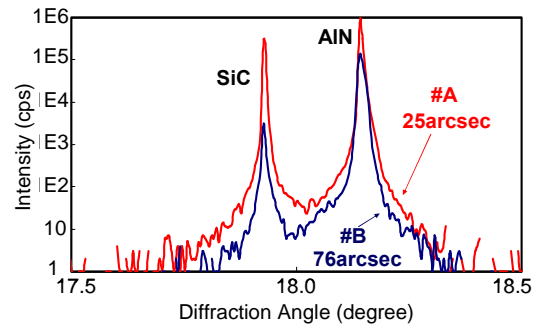


Fig. 12 X-ray diffraction spectrum (ω - 2θ) of AlN on n-SiC.

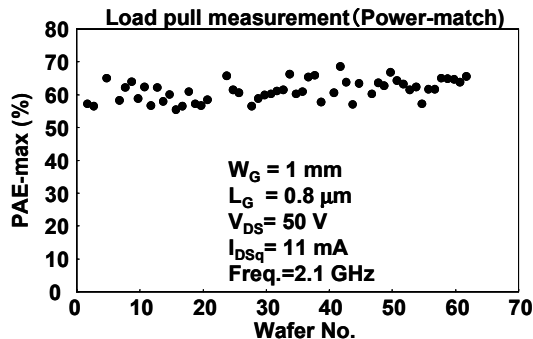


Fig. 10 Reproducibility of PAE among 60 wafers

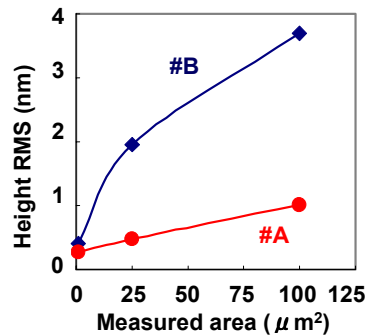


Fig. 13 RMS of GaN-HEMT on different AlN on SiC in Fig. 12. AFM scanned area was varied.

Table 1 Summary of the effect of AlN quality on GaN-HEMT.

	S.I.	#A	#B
Pout (W/mm)	5.2	5.2	3.1
PAE (%)	63	56	51
Current Collapse	Small	Small	Large
AlN FWHM (ω scan)(arcsec)	---	280	970
AlN FWHM (α -2 θ) (arcsec)	---	25	76
GaN FWHM (α -2 θ) (arcsec)	31	39	42
RMS @1 μm^2 (nm)	0.16	0.27	0.41
RMS @25 μm^2 (nm)	0.22	0.48	1.95
Mobility (cm ² /V/s)	1750	1670	1610

To transfer this technology for manufacturing, a 3-inch substrate should be used. Bow is an important issue to be checked when large diameter wafers are used. Bow was 8.7 μm even after MOVPE growth of GaN-HEMT structure on the AlN buffer layer. This is sufficient to obtain a fine 0.8 μm -long gate. Threshold voltage (V_{th}) and transconductance (g_m) of AlGaIn/GaN HEMT were -1.55 V and 194 mS/mm across an entire 3-inch conductive SiC substrate. Standard variations of those values were 0.15 V and 3.9 mS/mm. The 1-mm-gate-periphery GaN HEMT chip, which was operated at 60 V, achieved high CW output power density of 7.0 W/mm, with a high linear gain of 22.2 dB and power added efficiency (PAE) of 70% at 2.14 GHz. Standard variations of power density, linear gain and PAE at 50 V were only 0.42 W/mm, 0.2 dB and 3.0 point, respectively (Fig. 14). This low-cost highly uniform high-gain chip technology is sufficient for mass production of wireless base station application using GaN-HEMTs.

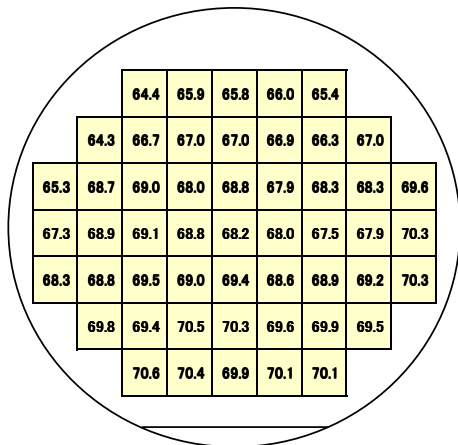


Fig. 14 PAE distribution across an entire 3-inch n-SiC substrate.

4) GaN-MIS-HEMT [6]

No report of over 100 W GaN-MIS-HEMT is attributable to the fact that the semiconductor surface in contact with the insulation layer used a layer of AlGaIn, which contains aluminum. Aluminum oxidizes easily, which leads to degradation of performance.

Our developed transistor consists of silicon nitride deposited on the outermost layer of a GaN-HEMT epitaxial layer that has a thin film of n-type doped GaN (Fig. 15). By using a GaN layer, instead of an AlGaIn layer, oxidation of the surface could be prevented. As a result, maximum output of 110 W with no forward gate leakage was achieved (Fig. 16). This is the first insulated gate transistor capable of producing output of over 100W. In conjunction with the digital pre-distortion circuits that are essential for base station amplifiers, low adjacent channel leakage power was also confirmed.

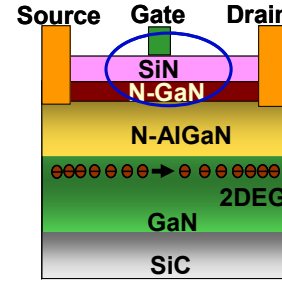


Fig. 15 Schematic cross sectional view of AlGaIn/GaN MIS HEMT with surface-charge-controlled n-GaN-cap structure.

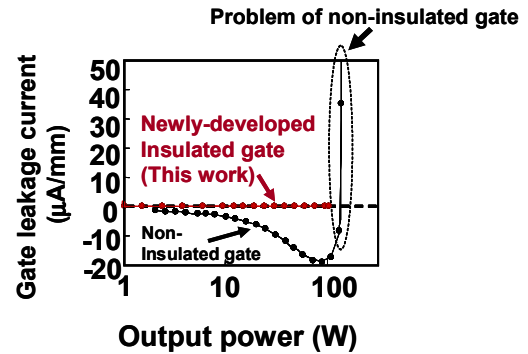


Fig. 16 Gate leakage current of over 100 W GaN-HEMTs using (a) Schottky gate and (b) MIS gate.

CONCLUSIONS

Reliability phenomena of GaN-HEMTs were addressed. Effect of the hexagonal pits on yield is discussed. Low cost solutions were introduced considering thermal handing. Newly-developed MIS-HEMTs which could be operated at 60 V with 110 W were also reported. These results show promise of GaN-HEMT in the future wireless infrastructure market.

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REFERENCES

- [1] T. Kikkawa, Japanese Journal Appl. Phys., 44 (2005) pp. 4896-4901.
- [2] T. Kikkawa et al., 2001 IEDM Tech. Dig., pp. 585-588.
- [3] M. Kanamura et al., 2004 IEDM Tech. Dig., pp. 799-802.
- [4] T. Kikkawa et al., 2005 CS-IC Tech. Dig., pp. 77-80.
- [5] K. Imanishi et al., IEICE Tech Dig. (in Japanese) Kanazawa, June, 2005.
- [6] M. Kanamura et al., 2005 IEDM Tech. Dig.
- [7] T. Kikkawa et al., to be published in IEICE Transactions (2006).