An Ion-Implanted GaAs MESFET Process for 28V S-band MMIC Applications

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Abstract

As an extension of M/A-COM's 10V MSAG™ power process, we have demonstrated an ion-implanted, MMIC-compatible, GaAs MESFET (HVMSAG™) that utilizes a gate-connected field plate to enable improved high voltage operation. This high-voltage FET is capable of 1.5W/mm P_{out} and 60% PAE at S-band, operating from a 28V drain supply. The HVMSAG process has demonstrated four important features: proven reliability at 28V, full MMIC capability with demonstrated power scalability, low cost, and immediate production capability.

INTRODUCTION

There are many benefits derived from operating RF and microwave power amplifiers at bias voltages as high as possible. Such benefits include increased power per unit size, lower I^2R losses in the system, and easier, more efficient matching at the output. For example, where a semiconductor-device solution is possible (e.g., base-stations for cell phones), high-voltage silicon power FETs have long been the device of choice for high-power RF applications. Demands from emerging commercial applications and next-generation military applications for higher power, frequency and efficiency have created tremendous interest for developing compound-semiconductor-based power amplifiers capable of operating at 28V and above. Much development has focused on using wide-band gap (WBG) semiconductors such as SiC and GaN [1,2] whose materials properties readily allow high-voltage operation and provide high power density at RF *and* microwave frequencies. However, these device technologies are immature, with many problems remaining to be solved before full-scale production can proceed, not the least of which is the high cost and limited availability of substrate material [3]. Simultaneously, some companies are pursuing GaAs-based power FET technologies, for RF and microwave applications, which can operate at voltages as high as 28V [4-9]. Although GaAs-based HV power devices do not offer the same levels of power density as demonstrated by WBG technologies, they typically have the advantage of being an extension of proven, manufacturable technologies.

M/A-COM has developed an ion-implanted GaAs MESFET process that utilizes a gate-connected field plate to enable high voltage operation of a power FET in discrete or MMIC applications. This high voltage GaAs MESFET (HVMSAG) process is an extension of M/A-COM's 10V MSAG power process. The HVMSAG MESFET (or HVMFET) is capable of 1.5W/mm P_{out} and 60% PAE at S-band, operating from a 28V drain supply. An important distinction of the HVMSAG process over devices fabricated from WBG materials is that HVMFETs are based on an existing, mature GaAs MMIC power process with proven reliability. The HVMSAG process is currently in production and has demonstrated four important features when compared to WBG technology: proven reliability at 28V, full MMIC capability with demonstrated power scalability, low cost, and immediate production capability. Arrhenius-plot accelerated life test results for HVMFETs predict MTTF of $>10^6$ hrs at 150°C channel temperature showing that, at 28V, the HVMSAG process is extremely robust against thermally activated failure mechanisms.

In this paper we show results of the HVMFET development effort, HVMFET characteristics (including dc, RF-small signal, load pull, and reliability), process vs device correlation results, process control, and summary results for a small-scale S-band MMIC HPA production run.

HVMFET DEVELOPMENT

The HVMFET is based on the MSAG process, which is an ion-implanted, planar-MESFET, MMIC-compatible process. The selective implant process approach and planar structure of the basic MSAG FET, with its self-aligned features and refractory-gate-first process sequence, allows tremendous freedom and flexibility of device design and device optimization. An additional benefit of the MSAG process approach is the ability to include, in the same circuit, FETs individually optimized for power, low noise, switching, and digital functions [10]. Thus, design of an HV power FET (see HVMFET cross section drawing below)

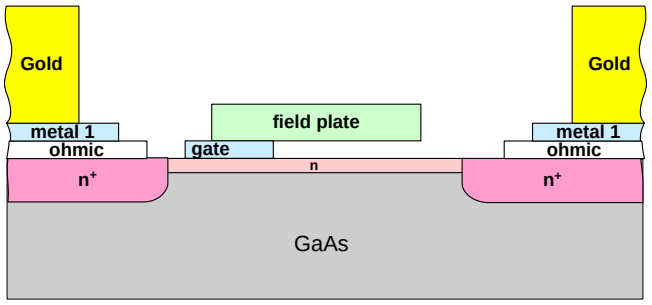

Figure 1. Cross section drawing of HVMFET showing Gate-Connected Field Plate (GCFP). Region under the field plate is filled with passivation dielectric.

was relatively straightforward, particularly so after developing and patenting the gate-connected field plate which is a simple extension of the gate overlay metal already in use on standard MSAG power FETs. The prototype HVMFET investigation was followed by a device optimization effort which focused on power and efficiency for S-band MMIC applications. This effort consisted of empirically evaluating device-design factors such as gate length, field-plate dimension, source-drain spacing, implant energies, implant doses, etc.

A mask with a full-factorial layout of FETs, covering all critical-dimension variants, was used in the study. Process factors such as implant energy and dose were varied wafer-to-wafer in process lots. A total of over 400 device variants were produced, and tested dc and small-signal RF. Based on these results, the most promising candidate FETs were pursued and evaluated with load-pull measurements. The dc and small-signal RF measurements and analyses were facilitated by software developed in house for automating on-wafer test and data storage. Much of the analysis was performed using the powerful statistical analysis software JMP from SAS. From this study, an HVFET was chosen that best satisfied all the criteria for power performance in an S-band MMIC at 28V drain bias. The chosen FET was thoroughly characterized and released for production.

HVMFET Characteristics

Figure 2 shows typical values for key dc FET parameters and Equivalent-Circuit-Model RF parameters derived from 24V S-parameter measurements of a 450µm HVMFET. Load-pull data is shown for the HVMFET in Figure 3. Maximum P_{out} at S-band frequencies is typically 1.5W/mm at 28V drain bias. With the gate-overlay feature of the MSAG process, the increase in BV associated with the GCFP is readily seen. In-process tests routinely performed on HVMFETs before and after the GCFP is fabricated show an average increase in BV of about 9V and the unexpected benefit of reduced variability in BV, as shown in Figure 4. The HVMFET was also characterized for ruggedness under operating conditions of severe mismatch. Figure 5 shows excellent survivability under such conditions.

RF Parameters (at 24V V_{ds})			dc Parameters (at 1.8V V_{ds})		
	Value	**Units**		**Value**	**Units**
Gm	54	mS/mm	I_{peak}	325	mA/mm
Cgs	1920	fF/mm	V_t	-3.4	Volts
C_{gd}	47	fF/mm	BV_{gd}	56	Volts
R_{ds}	530	Ohm*mm			
f_T	4.7	GHz			

Figure 2. RF and dc target values used for in-process monitoring of the HVMFET.

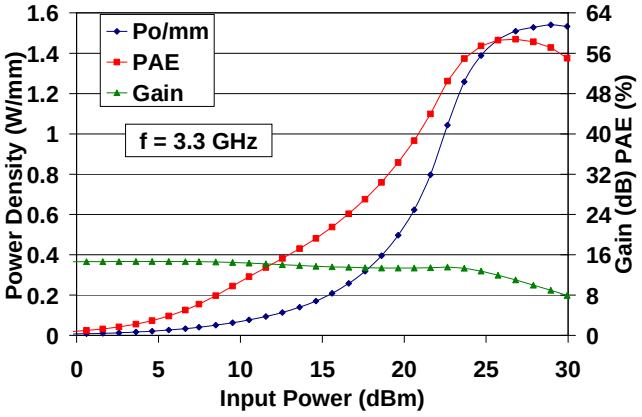

Figure 3. Typical load-pull results measured at 3.3 GHz for a 4mm HVMFET at 28V drain bias. Tuned for power, maximum output power density is typically 1.5W/mm with PAE up to 60%.

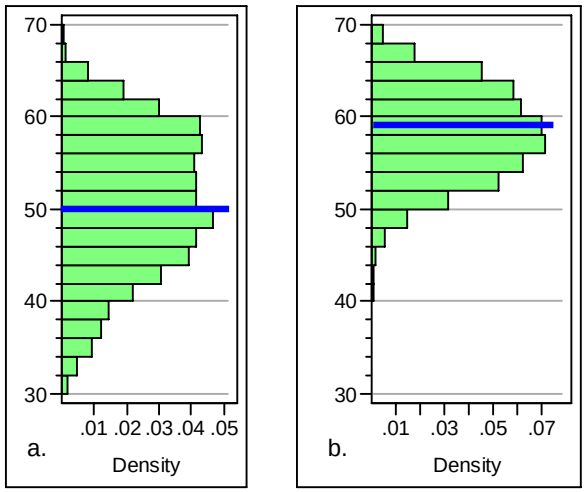

Figure 4. HVMFET breakdown voltage (vertical scale) distribution from production wafers tested (a) before and (b) after the GCFP is applied. The FP produces a typical increase in BV of about 15% and also reduces BV variability wafer-to-wafer by 60%.

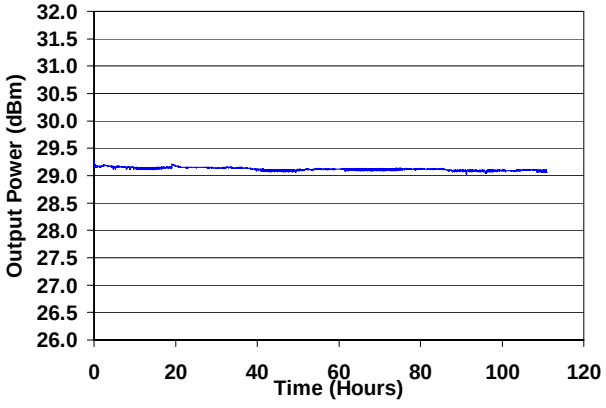

Figure 5 Output power stability of a 4mm FET with 10:1 load mismatch at drain bias of 30V. Power changed less than 0.1 dB over the duration of the test.

Past experience with other MSAG FETs has shown diffusion/migration of ohmic metal to be the primary thermally activated failure mode. Accelerated-life tests of the HVMFET gave similar results, but with a predicted MTTF even longer than for other MSAG FETs, as might be expected for a device with larger electrode spacings, for this failure mode. An Arrhenius plot comparing results for the 10V MSAG FET and the HVMFET is shown in Fig. 6.

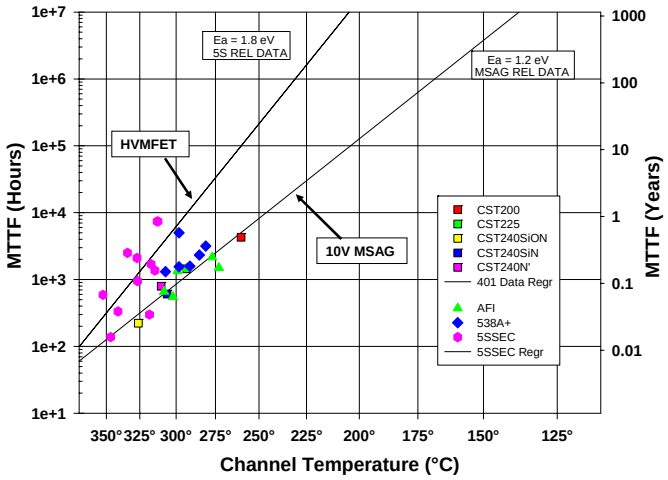

Figure 6. Arrhenius plot for the temperature-accelerated life test data shows extrapolated MTTF of > 10^7 hours at 150°C for the HVMFET.

MULTIVARIATE MODEL (MVM)

A quantified understanding of the relationships between device dimensions, process parameters and device electrical characteristics is a valuable asset for the manufacturing engineer in his efforts to control processes for achieving high yields to PCM and circuit performance specifications. In prior work which focused on the 10V MSAG power FET, we reported on the MVM approach [11], an empirical method for obtaining such process vs device information. For the HVMFET, an MVM was developed based on the assumption of linear, non-interacting relationships between FET electrical characteristics (Ip, Gm Cgs, etc.) and FET-process/design factors (channel implant, anneal temperature, Gate CD, etc.). Such a model approximation is valid only over small ranges of factor values and is therefore not very useful for performance extrapolation. However, it is extremely useful for a better understanding of key factors that can produce variability in FET characteristics in the manufacturing process and therefore, it is useful as an aid in process control. The form of the model equation is:

$$Z_i = K_i + S_{ai}A + S_{bi}B + S_{ci}C \ldots.$$

Where Z_i represents a FET electrical parameter (e.g., dc I_{peak}), A represents a FET process or design factor (e.g., channel implant dose), and S_{ai} represents the sensitivity of parameter Z_i to factor A. The full model consists of an array of S values over all factors investigated. In this effort, we developed an MVM model using multiple 8-wafer process lots covering key process factors and using a mask containing test FETs covering several dimensional factors and levels. Figure 7 summarizes the MVM S-matrix produced in the initial MVM study for the HVMFET. Over 9000 FETs were measured in generating the finished MVM.

		Z_1 (BV)	Z_2 (Ip)	Z_3 (Vt)	Z_4 (Gm)	Z_5 (Cgs)	Z_6 (Cgd)	Z_7 (Rds)	Z_8 (Ft)	Z_9 (pIm)
Factors		Sensitivities								
Implant 1	**A**	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	S_{a9}
Implant 2	**B**	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	S_{b7}	S_{b8}	S_{b9}
Anneal T	**D**	S_{d1}	S_{d2}	S_{d3}	S_{d4}	S_{d5}	S_{d6}	S_{d7}	S_{d8}	S_{d9}
Dielectric	**F**	S_{f1}	S_{f2}	S_{f3}	S_{f4}	S_{f5}	S_{f6}	S_{f7}	S_{f8}	S_{f9}
CD 1	**G**	S_{g1}	S_{g2}	S_{g3}	S_{g4}	S_{g5}	S_{g6}	S_{g7}	S_{g8}	S_{g9}
CD 2	**H**	S_{h1}	S_{h2}	S_{h3}	S_{h4}	S_{h5}	S_{h6}	S_{h7}	S_{h8}	S_{h9}
CD 3	**I**	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	S_{i7}	S_{i8}	S_{i9}
CD 4	**J**	S_{j1}	S_{j2}	S_{j3}	S_{j4}	S_{j5}	S_{j6}	S_{j7}	S_{j8}	S_{j9}
K Factor		K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9

Figure 7. Layout of sensitivity-factor array for HVMFET MVM. Test results included a full range of device parameters, but only Pass-Fail PCM parameters, as shown here, were used for generation of the MVM.

As an example of the MVM results, Figures 8 and 9 show measured vs MVM-predicted values for Ipeak and BV. Confirmation runs have validated MVM sensitivity factor values for key FET parameters to be accurate to within approximately 10%. With knowledge of process-factor variation, the MVM can be used to predict yield vs PCM specifications and as and aid in prioritizing areas of process improvement based on a yield-benefit assessment.

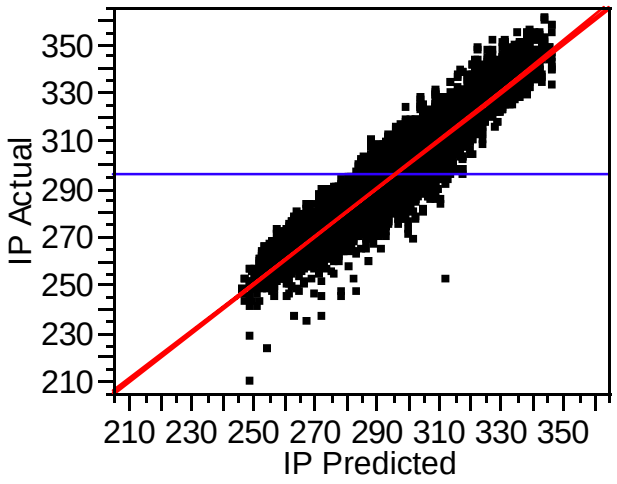

Figure 8. Example of multivariate least-square fit showing that the MVM prediction matches measured values of Ipeak with an R^2 fit of 0.88. The MVM prediction for BV matches measured values with an R^2 fit of 0.92.

PRODUCTION RESULTS

We have processed over 800 4-inch wafers during the development, pre-production, and a recent small-scale production build of S-band HPAs. Figure 9 shows run-chart

wafer-average dc-Ipeak data for standard-process HVFET wafers over this time period. In production, wafer-wafer and across-wafer standard deviation of HVMFET Ipeak is 12 mA/mm (3.7%) and 5.4 mA/mm (1.7%), respectively.

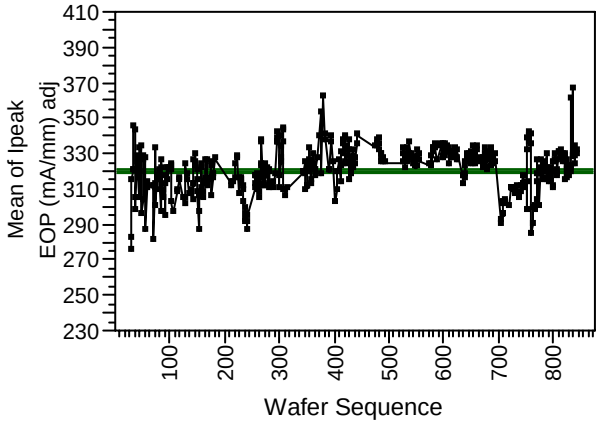

Figure 9. Run chart of Ipeak for standard-process HVMFET wafers. The median wafer-average value of Ipeak is 321 mA/mm and the standard variation wafer-wafer is less than 4%.

Using the HVMSAG process, a small-scale production build of S-band HPAs was initiated, and to date, over 300 wafers have been fabricated in this build. In addition to the HVMSAG FET, other features of the MSAG process were taken advantage of in order to achieve the very high power requirements for the circuit. For example, Multi-Level-Plating (MLP), a process which produces two global layers of 4.5µm thick plating was used to facilitate power handling in the circuit and reduce losses in matching elements on the circuit, and also in a combined 9µm thick double-layer for high-current busses on the drain supply. Figures 10a and 10b, histograms of P_{out} and PAE for the S-band HPA for over 10,000 circuits tested on-wafer, show tight distribution of power performance using the HVMSAG FET.

CONCLUSION

As an extension of M/A-COM's 10V MSAG power process, we have demonstrated an ion-implanted, MMIC-compatible, GaAs MESFET that utilizes a gate-connected field plate to enable improved high voltage operation. This high-voltage FET is capable of 1.5W/mm P_{out} and 60% PAE at S-band operating from a 28V drain supply. The HVMSAG process has demonstrated four important features: proven reliability at 28V, full MMIC capability with demonstrated power scalability, low cost, and immediate production capability.

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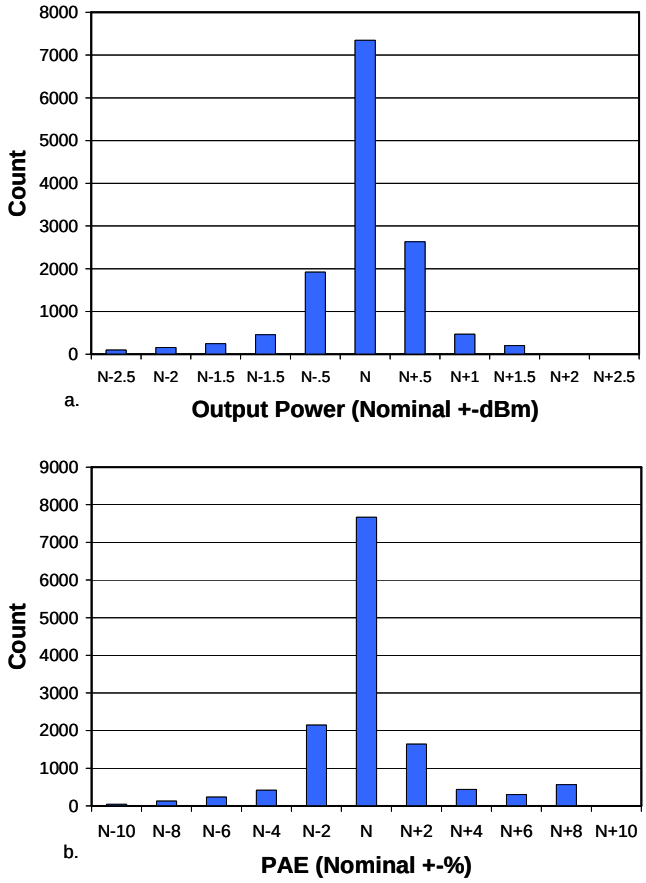

Figure 10. Wafers from a production run of S-band HPA MMICs were on-wafer tested at 24V for P_{out} and PAE with the results for the center-band-frequency performance shown above for over 10,000 dc-good die. Nominal P_{out} and PAE are in excess of 40W and 18% respectively for this S-band HPA which demonstrates > 30% bandwidth. Tight distributions like these give rise to the high circuit yields and associated affordable costs needed for practical implementation of high-voltage MMIC technologies.

REFERENCES

[1] L. Larson, P. Asbeck, and D. Kimball, *2005 IEEE CSIC Symposium Technical Digest*, pp. 1-4 (2005)
[2] D.C. Streit, A. Gutierrez-Aitken, M. Wojtowitz, and R. Lai, *2005 IEEE CSIC Symposium Technical Digest*, pp. 5-8 (2005)
[3] M. Rosker, *2005 IEEE CSIC Symposium Technical Digest*, pp. 13-16 (2005)
[4] C.-G. Yuan, et.al, *2005 CS MANTECH Conference Technical Digest*, pp. 27-30 (2005)
[5] B. Yang, et.al, *2005 IEEE CSIC Symposium Technical Digest*, pp. 244-247 (2005)
[6] M. Miller, *2005 CS MANTECH Conference Technical Digest*, pp. 236-239 (2005)
[7] B.M. Green, et.al, *2004 IEEE MTT-S Digest*, pp. 817-820 (2004)
[8] H. Haematsu, et.al, *2005 CS MANTECH Conference Technical Digest*, pp. 39-42 (2005)
[9] T. Winslow, *2005 IEEE CSIC Symposium Technical Digest*, pp. 240-243 (2005)
[10] E.L. Griffin, *2000 IEEE MTT-S Digest*, pp. 709-712 (2000)
[11] D. Miller, *2003 GaAs MANTECH Conference Technical Digest*, pp. 139-142 (2003)