Defect Reduction in Through Wafer Via Photolithography Processing

J. Riege, T. Nguyen, H. Knoedler, B. Darley, R. Clark, N. Ebrahimi, S. Mony, S. Tiku

Skyworks Solutions, 2421 West Hillcrest Drive, Newbury Park, CA 91320
jens.riege@skyworksinc.com (805) 480-4434

Keywords: Through Wafer Via, Via Rings, Variable Viscosity Resist

Abstract

As customer requirements reduce the maximum product defects allowed to less than one part-per-million, identifying the source of the occasional defect during wafer processing becomes more challenging. We observed a defect on wafers we call "via rings". This defect occurs when the street photoresist does not sufficiently protect the plated gold film at the top edge of the through wafer vias during the street etch process. This paper discusses the use of an additional step during the street resist coat process to ensure that the resist properly protects the edges of the vias during the etch process.

INTRODUCTION

Coating a wafer with topography with a thick photoresist to protect large features from etching is not a challenging task. It is challenging, however, to use a viscous resist and not leave any bubbles in millions of 100 µm deep via holes (See Fig I). A bubble can pop or its outer resist shell can erode in subsequent processing steps. Even if bubbles remain intact the likelihood of via etch attack increases with the increase in the number of vias with bubbles (see Fig. II). The solution presented in this paper reduces the presence of bubbles inside the vias significantly so that etched via defects occur in less than one via per billion. The fundamental principles behind this idea can be applied to other processes that coat a viscous polymer over steep topography.

PROCESS OVERVIEW

When wafer processing is complete on the front side of a GaAs wafer used to make HBT power amplifier circuits, processing continues on the back of the wafer. The backside process etches vias from the back of the wafer through to front side metal connections, and then plates a film of gold over the entire backside of the wafer and in the vias.

To protect the front side of the wafer from damage during backside processing, it is first mounted front side down onto a sapphire carrier using an adhesive polymer or wax. A grinding process thins the wafer until it reaches the desired final thickness. The wafer goes through a photo-lithography process step that defines the pattern for tens of thousands of via holes that will be dry-etched through the wafer. The photoresist used at this step must be thick enough to protect the unpatterned area of the backside of the wafer during the dry etch process. After the via etch is complete and the resist is removed, a NiV\Au[1] seed layer is deposited on the back of the wafer. Next the wafer is plated with a few microns of gold on the entire backside of the wafer as well as inside the vias.

To electrically isolate each die a photolithography step patterns a "street" border around all die and the wafer is etched in a gold etch solution. Our street pattern process

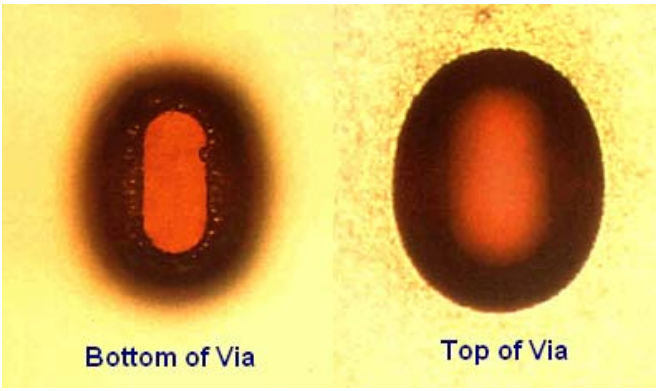

FIGURE I
THROUGH WAFER VIA COMPLETELY FILLED WITH RESIST.
BOTTOM OF VIA IS CLEARLY VISIBLE.

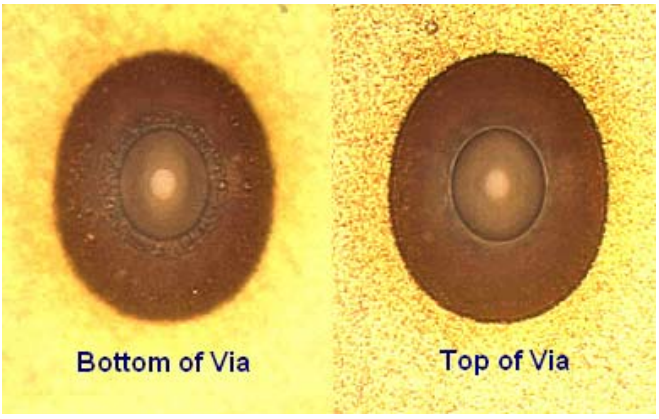

FIGURE II
THROUGH WAFER VIA WITH BUBBLE IN RESIST COATED VIA.
BOTTOM OF VIA IS OBSCURED BY BUBBLE.

uses the same resist used in the via coat process. The resist coats the back of the wafer but must now fill the 100 µm deep etched vias.

It is easy to see when vias are filled with resist completely by focusing at the top and the bottom of a single via after coat or develop (See Figures I and II). If the via bottom is opaque or not clearly visible, a bubble is present.

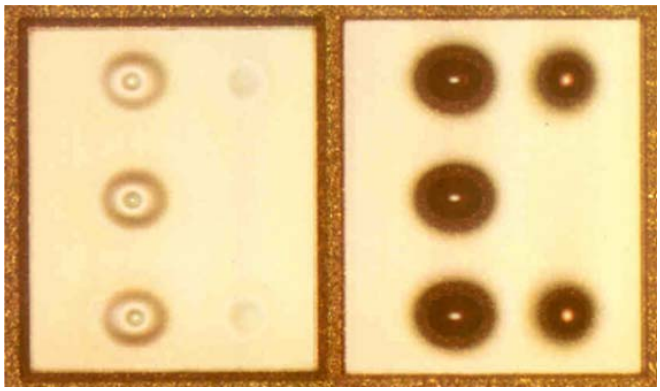

FIGURE III
DIE WITH FIVE VIAS:
WITH (LEFT) AND WITHOUT BUBBLES (RIGHT)

Vias filled with resist show the bottom via surface clearly and magnified by the concave top surface of the resist. Fortunately for the operator, bubbles are easy to see with a low power microscope (See Figure III). Vias with bubbles appear much lighter in color. When photoresist fills vias completely, the vias absorbed most of the incident light and appear dark.

Wafers are baked on a hotplate to remove the excess solvent and harden the photoresist and are then exposed and developed to form the street border around each die. The gold etch process then removes the gold in the street border, and the resist is stripped from the wafer.

After backside processing is complete, the wafer is heated on a hotplate to soften the wax or polymer so that it can be demounted from the sapphire carrier. When the wafer has cooled it is cleaned in a solvent bath. The wafer is electrically tested, scribed, and broken to separate each die for inspection and final assembly.

PROCESS PROBLEM

At the street coat process any via that is not filled with photoresist contains air. The trapped air forms bubbles whose size, integrity, and location depend upon subsequent processing steps. After resist coat the wafer is baked on a hotplate and bubbles in the vias expand rapidly. The resist around the bubble thins as seen by rings of refracted light at the top of some bubbles. This thinner resist is more likely to erode in the next processing steps, such as develop. During develop a small amount of unexposed resist is lost under normal processing conditions, also known as dark film loss. The loss of resist occurs because a small percentage of light passes through the chrome in the mask along with stray light reflections from the aligner optics to expose the unexposed regions of the wafer. When the top of the bubble is developed, the dark film loss can cause the top of bubble to form a hole (See Figure IV). In some cases the hole can release stress and the resist will crack.

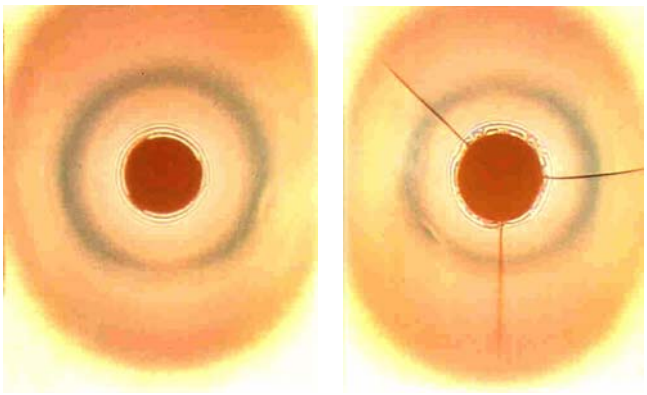

FIGURE IV
ELLIPTICAL VIAS WITH HOLE AND WITH CRACKED HOLE

The outer bubble shape is convex, making it the highest topography on the wafer if we ignore the bead of resist found at the edge of the wafer. Any accidental contact with the bubble can break the surface and open the bubble. During the street gold etch, the etch solution can enter this hole. When the bubble touches the inside edge of the via the resist offers little protection to the plated gold and increases the possibility that the gold will be etched.

To detect via rings operators perform a 100% wafer inspection after the street etch is complete. Since the NiV seed layer appears silvery white compared to the plated gold, via rings, if present, stand out in sharp contrast and are easily detected (See Figure V).

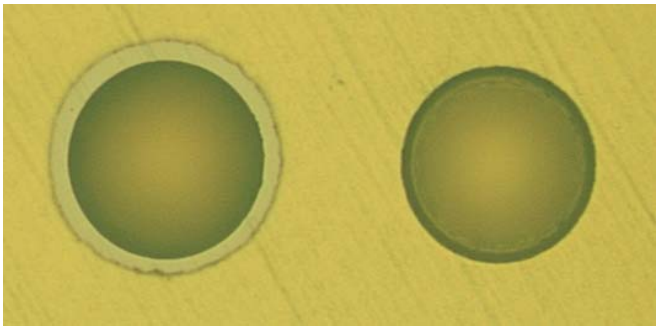

FIGURE V
THROUGH WAFER VIA AFTER STREET ETCH:
WITH VIA RING (LEFT) AND WITHOUT VIA RING (RIGHT)

Unfortunately, this inspection methodology is not sufficient to identify all incidences of via rings. SEM

micrographs showed that some etch attack is so light that it is not detectable under a microscope (see Figure VI).

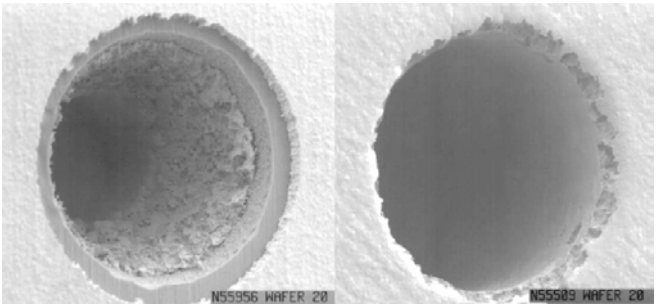

FIGURE VI
SEM MICROGRAPH OF TWO VIA RINGS:
DETECTABLE (LEFT) AND NON-DETECTABLE (RIGHT)
DURING OPTICAL MICROSCOPE INSPECTION

A second method of detection uses an electrical resistance test performed on Process Control Monitors (PCM). If via rings occur in die outside the PCM the electrical resistance probe tests cannot detect them. Therefore, a complete solution to getting rid of via rings requires getting rid of the bubbles in the vias.

PROBLEM HISTORY

Our original theories on how via rings occurred assumed bubbles formed due to resist outgassing nitrogen. Outgassing is a process in which photoresist liberates nitrogen gas when exposed to UV light. High light intensity during wafer exposure heats the resist and accelerates nitrogen diffusion to the resist surface. We speculated that if the outer resist surface is hardened during the bake after coat, the gas can be trapped and a bubble can form during wafer exposure. Early observations detected bubbles during inspection after develop.

Bubbles were also detected the instant wafers made contact with the hotplate after coat. Changing this bake process to a proximity bake and slowing the bake temperature ramp reduced the incidence of bubble formation, but did not eliminate them. Similarly, dropping the hotplate temperature and extending the bake time did not prevent them from forming.

After tracing the source of via bubbles by process step from etch back to coat, a direct inspection of vias verified that small bubbles first appear during resist coat before bake. No bubbles exist in the resist coating on the wafer surface around the vias or when coating flat wafers in the via coat process, so neither the photoresist nor the dispense process supplies the bubbles.

Another factor considered as a cause of via rings was via size. Inspection of different sized vias on test structures found bubbles in much larger as well as smaller vias, suggesting that size was not the primary factor for bubble formation. This was fortunate for us since product design rules did not permit us to change the via size.

Bubbles were also detected at coat before the resist was baked which left little time for gases to diffuse to the resist surface. We concluded that the probable source of the bubbles was the high resist viscosity preventing improper resist filling of the vias. Subsequent efforts addressed resist viscosity as the potential source of via rings.

PROBLEM SOLUTION

One solution to try to eliminate via rings could be to evaluate a lower viscosity resist. However, to save cost we had the added constraint of using the same resist used at the via coat process. Since the via resist process requires a resist coating at least 17 μm thick, a single coat of a low viscosity resist cannot be used for both the via and street processes.

Another solution was to coat wafers twice, something we used in the past. At that time we detected via rings near the edge of the wafer, so this process was not a complete solution. Going back to a double coat process would cut our tool capacity in half, would use twice as much resist and double the cost of the resist used. Since a two-coat process was more expensive and did not ensure bubble-free coatings we chose not to pursue this option.

Our solution was to create a variable viscosity resist by pre-wetting the wafer with solvent just before resist dispense. Before the solvent dried, we dispensed photoresist and allowed the resist to mix with the thin solvent film on the wafer. As the resist spread to the edge of the spinning wafer it mixed with the solvent and its initial viscosity dropped. The viscosity of the resist coating on the wafer then increased as the dispensed resist consumed the solvent. The final viscosity of the resist was high enough to permit us to reach our existing resist thickness target with a small spin speed reduction during the coat recipe resist thickness casting step. While it is now common to use a solvent on wafers before resist dispense to help reduce resist usage[2], it is not typically used to mix with the photoresist directly.

PROCESS VARIABLES

We identified five factors that significantly affect bubble formation. Three ensure the wafer remains wet with solvent before the resist is dispensed. The time between solvent dispense and resist dispense is critical. The spin speed after solvent dispense affects the evaporation rate of solvent left on the wafer. Air flow around the wafer during solvent dispense is the third factor, but due to our coat track design we could not adequately control this variable. The first two factors were within our control and significantly affected the amount of solvent available to mix with the resist. To optimize the resist coat process, the spin speed after solvent dispense was adjusted to minimize bubbles in vias on the wafer and at the same time have the lowest resist thickness variation. Increasing the spin speed reduces resist thickness

variation but increases bubble formation. Decreasing the spin speed leaves only a few bubbles in the vias but generates high resist thickness variability due to a non-uniform viscosity of the resist (See Figure VII). Variation in resist viscosity across the wafer will generate higher thickness variation as the solvent evaporates.

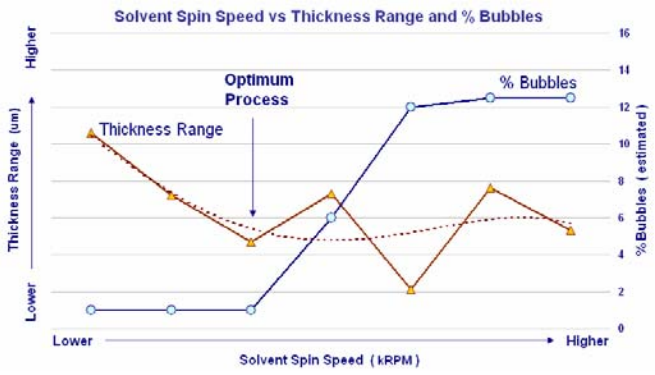

FIGURE VII
SPIN SPEED DURING SOLVENT DISPENSE VS. BUBBLE FORMATION AND RESIST THICKNESS UNIFORMITY

The fourth critical factor is via shape. Most of our products have vias etched with a tapered top edge profile, similar to the shape of a Martini glass. A few of our products have vias with near vertical sidewalls. When these products use the new coat process they still have many bubbles in the vias and two wafers had via rings. Experiments that thinned the resist further by leaving more solvent on the wafer and slowing resist dispense spin speed did not sufficiently reduce bubbles and worsened coating uniformity. Our solution to try to eliminate via rings from these products will be to convert them to the tapered via design.

A fifth factor to bubble formation was wafer cleanliness. In an experiment using uncleaned wafers after wafer grind, bubble formation was severe, even though the wafers went through via resist coat, via etch, via resist remove, plasma ash and plating processes. These results show that via rings can be formed if the regular wafer cleaning process after wafer grind is omitted or is marginal.

The general appearance of the new street coat process is noticeably different than the standard process. The shape of the leading edge of the resist wave had a shallower contact angle compared with the non-diluted resist coat process. This angle change indicated that the lower viscosity resist wetted the wafer more effectively and provided potentially better resist adhesion compared with the non-diluted resist.

WAFER YIELD

We estimate that via rings impacted wafer yield at a level of approximately one via ring per million using our standard resist coat process. This process left wafers with approximately 95% of the vias filled with bubbles. Using the pre-wet/mixing process, the number of vias with bubbles was reduced to 1 - 5%, and via rings have not yet been found on non-vertical wall vias. After several months of no via rings, the defect rate is at the one via per billion defect level.

CONCLUSIONS

We have observed that bubbles left in through wafer vias at the street photoresist coat step can generate via rings at a one part-per-million defect level. When a bubble pops it increases the risk that the street gold etch process will attack the gold plated edge of the via and form via rings.

By applying a solvent to a wafer and allowing the resist to mix with it before it dries, it is possible to generate a resist with a variable viscosity. The lower initial viscosity improves the resist's ability to fill deep vias completely. Solvent/resist mixing can be controlled by adjusting spin time and spin speed between solvent dispense and resist dispense. The optimum process minimizes bubble formation in vias and maintains resist thickness uniformity.

When vias are completely filled with resist, the existing path for the etch attack of the plated gold film has been removed, reducing the device defect level to one part-per-billion level or less.

ACKNOWLEDGEMENTS

The authors would like to thank Dennis Anderson, formerly of Skyworks Solutions, for his effort in identifying via rings and his preliminary investigations into their cause.

REFERENCES

[1] H. Knoedler, et al, *Cross-functional Optimization of Backside Metal Adhesion to GaAs*, 2005 CS MANTECH Technical Digest, pp. 89-92.

[2] B. Lorefice, et al, *How to Minimize Resist Usage During Spin Coating*, Semiconductor International, June 1, 1998, at http://www.reed-electronics.com/semiconductor/article/CA164074?

ACRONYMS

HBT: Heterojunction Bipolar Transistor
TWV: Through Wafer Via
PCM: Process Control Monitor