# Substrate Via Etch Profile Optimization using RIE and Wet Etch Processes

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**Abstract:**

**This paper provides a summary of the development of a robust substrate via process using a selective etch. The parameter space of an RIE etch process was investigated. It was found that under certain conditions, a via undercut can be observed. This was an unexpected result. The epitaxial layers of pHEMT material were found to be particularly sensitive. Controlled experiments identified a galvanic effect that enhanced lateral etching. The probability of cavity formation increased when frontside gold metal was exposed due to poor selectivity of the RIE process to the Ti and Pt layers on the frontside interconnect metal.**

## INTRODUCTION

A robust through wafer via process is essential for high volume GaAs manufacturing. Typically, these etch processes are optimized with respect to profile and overall etch rate. While optimizing these parameters addresses electroplated metal coverage and process throughput, there are other issues that deserve particular attention. For example, metal adhesion and the role of wet cleans within GaAs substrate vias has been studied [1]. Another concern is via undercut and void formation at the frontside metal interface and is the subject of this study.

Cavity formation can lead to reliability concerns due to trapped materials that outgas during heat cycling. The potential of this problem depends on the metal stack that is present where the via terminates. Substrate vias that terminate on source pads provide a robust interface, since the ohmic metal is alloyed into the substrate. In these cases, via undercut is not a primary concern. The process requirements are different, however, when via structures terminate on fronstide interconnect metal. These metals typically contain Ti, Pt and Au. The issue can be additionally troublesome when the substrate via terminates on the bottom plate of a MIM capacitor. With this particular structure, all via-metal interfaces must be especially robust. The added controls required for a process that provides a robust interface for all of these structures for a variety of via sizes can be challenging. Process throughput will likely be decreased.

## EXPERIMENTAL

The substrate via etch was performed in an AME8130 batch reactor. The RIE process consists of two steps. The first step is a non-selective etch utilizing $BCl_3$/ $Cl_2$ chemistry. This etch is performed under servo bias control and results in an etch rate of approx. 2.0 um/min. The second step employs $Cl_2$/F22 and is selective to the underlying AlGaAs layers. The selective process etches approximately 10 um of the remaining substrate thickness and stops on the epitaxial structure. Two etch process sequences were evaluated to etch the thin epitaxial layers to complete the process. One process utilized $BCl_3/Cl_2$ at low bias levels, while the other was a wet etch using $H_2SO_4$ and $H_2O_2$. The wet etch removes approximately 0.5 um of material and serves two requirements. First, the epitaxial layers are removed from the vias. Second, the etch removes any substrate damage from the grind process thus promoting good backmetal adhesion. The photoresist (approx 17 um) is removed prior to wet etch using a spray acetone process. This process also removes any polymer that may be present as a result of the etch.

## RESULTS

Lateral etching of the via sidewall profile at the substrate to metal interface was found to be most dependent on the effectiveness of the selective RIE etch process and the method of epitaxial layer removal. A pronounced lateral etch is observed after the damage removal etch when the via bottom was exposed to a nonselective process that removes the underlying Ti and exposes Au and/or Pt in the interconnect metal. We believe that this behavior is a result of electrochemical enhanced etching. This is observed after removal of the epitaxial layer using the aforementioned RIE process. To illustrate, a simple experiment was performed using epitaxial wafers with different etch masks. Each wafer was exposed to a wet etchant containing $H_2SO_4$ and $H_2O_2$. Figure 1 displays cross-sectioned results. The top left panel in Figure 1 is an example of the resulting profile when a resist

mask is used. As expected, a near isotropic profile is observed. The middle panel depicts the same process except a Ti etch mask is used. Here again, a near isotropic profile is observed. In sharp contrast, however, is the bottom panel when an Au mask is used. A dramatic lateral etch results that is roughly 10x the vertical rate. This phenomenon is observed on device vias as well. These cross-sections will be presented, but are not shown here. This undercut is not observed, however, when the experiment is repeated on wafers without epitaxial layers, such as the case with MESFET devices. Enhanced lateral etching at metal-GaAs interfaces has been previously reported [2]. In this referenced study, the investigators found unintentional etching of mesa structures during wet surface treatments when a metal mask was used. Recommendations included mask biasing as well as eliminating wet cleans when metals are exposed. This study did not examine the impact of changing the metal stack.

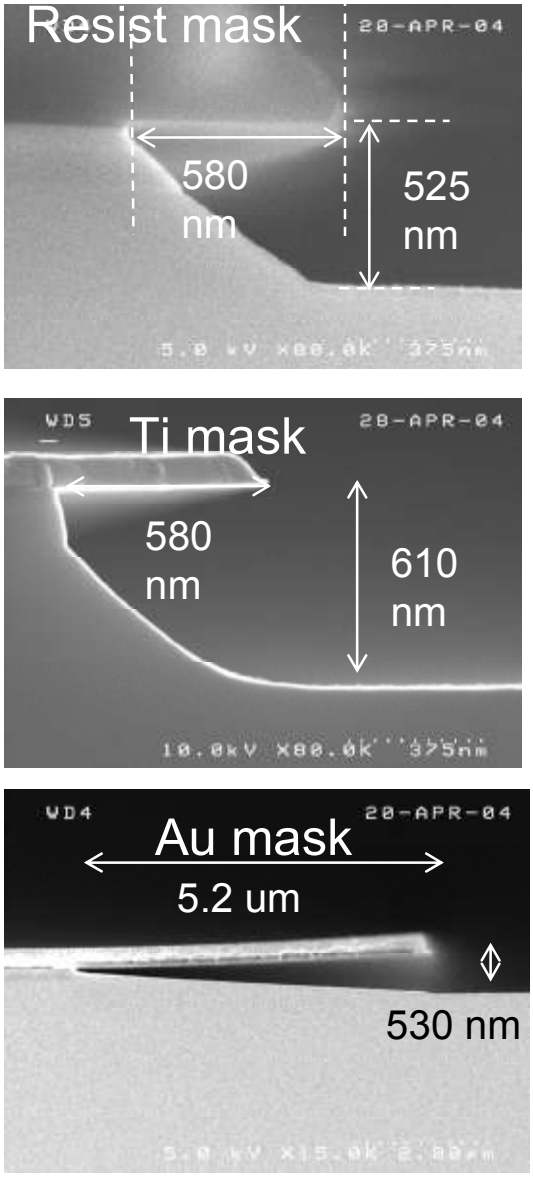


*Figure 1. Post wet etch SEM cross-sections on epitaxial pilots illustrating the galvanic etch mechansim that contributes to substrate via foot formation.*

An additional benefit of using a wet etch to complete the process is the resulting morphology at the bottom of the via. The processes are compared in Figure 2. As can be seen, the via prepared using the wet etch to removal of the epitaxial layers is much smoother than the via etched with the dry nonselective process. We have found that this morphology can be beneficial for downstream process integration.

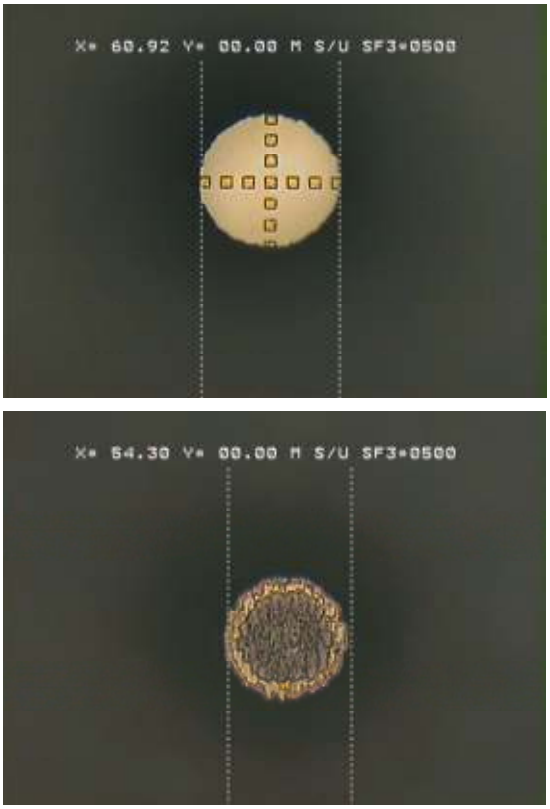


*Figure 2. Optical images of completed vias. Top panel: Example of a via completed using a wet etch. Bottom panel: This via was completed using nonselective RIE chemistry.*

## DISCUSSION

The observed undercut could be explained by examining the cathodic properties and cell potential of Ti with respect to Pt and/or Au in a galvanic cell. In one case, the Au/Pt metal would likely act as a cathode and the AlGaAs as a sacrificial anode. In the second case, the Ti would serve as the anode. More likely, however, is the suppressed reactivity due to the formation of a thin oxide on the Ti surface. The importance of $TiO_2$ formation in controlling material undercut has been studied previously [3]. Here Ti oxides were formed when exposed to $H_2O_2$. This enabled long overetch without significant pattern degradation. In our system, the oxide is formed during the wet etch removal step. The contribution of Al in the epitaxial stack could also be the key difference with the behavior observed on pHEMT and MESFET structures. This is speculation at this time.

## CONTROLS

To achieve a consistent selectivity on the Al-containing epitaxial layer, the process reworks were optimized to favor the selective port of the RIE etch. In addition, a time limit was placed between the selective RIE process and the wet etch. This was done as a precaution to assure consistent initiation of the etch process. Finally, a light ash was also used to promote wetting of the surface during the final via wet etch step.

## CONCLUSION

A robust substrate via etch process that can be used for capacitor over via structures for pHEMT devices has been demonstrated. The etch process uses selective chemistry for the final RIE process to consistently stop on the Al-containing etch stop layers. The via etch is completed using a wet etch. The process developed from the investigation eliminates the galvanic component and consequently the potential of any lateral etch. This process results in no lateral etching at the metal interface and provides excellent backmetal adhesion both within and outside the via area.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] J. Campbell et al, GaAs MANTECH conference digest 2005.
[2] I. Hallakoun et al, GaAs MANTECH conference digest 2000.
[3] J. E. A. M. van den Meerakker, J. P. Metsemakers,a and J. B. Giesbers, J. Electrochem. Soc., Vol 149, No 5, 2002.

## ACRONYMS

pHEMT: pseudomorphic High Electron Mobility Transistor
MESFET: MEtal Semiconductor Field effect Transistor
RIE: Reactive Ion Etch
MIM: Metal Insulator Metal
SEM: Scanning Electron Microscope
F22: Freon 2,2