Development of Backside Process For Use With Solder Paste Die Attach

Jason Fender and Terry Daly

Freescale Semiconductor, Inc.
Tempe Fab
2100 E. Elliot Road, Tempe, AZ, 85284
480-413-3521; 480-413-5029
jason.fender@freescale.com; terry.daly@freescale.com

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Abstract

In this paper we describe methods used to modify backside metallization in order to accommodate a change in solder assembly applications. As a cost savings effort, one of Freescale Tempe Fab's gallium-arsenide (GaAs) product lines was to be lead-tin (PbSn) solder-attached using methods at a silicon assembly site. The change in assembly methods introduced the problem of PbSn mixing into our standard backside gold (Au) metallization (ground) from die edges. Use of nickel-vanadium (NiV) as a solder barrier combined with process modifications designed to seal die edges was required to eliminate Sn and Pb mixing with backside Au.

INTRODUCTION

GaAs devices, typically, are assembled using either epoxy or solder die-attach methods. Most low-cost applications, including handsets, use epoxy attach. Epoxy die attach is much simpler, requiring only standard backside metallization schemes, e.g., titanium (Ti) adhesion layer and gold (Au) are commonly used at Freescale Tempe Fab [1]. However, high power devices, e.g., PHEMT, require solder attachment for adequate heat transfer. The work presented here required PbSn solder attach to NiV/Au backside metal. For Ni/Au systems, or in our case NiV/Au, the exposed Au top layer is required for solder attachment and to prevent oxidization of the Ni surface that must form new compounds with the solder. The volume ratio of Au to Sn must be controlled to prevent formation of brittle $AuSn_4$ intermetallic that is known to cause reliability failures [2]. Dissolution of the top Au layer with PbSn is desirable, but if paths (defects) exist within the barrier layer, solder can pass through the barrier and mix with backside Au. Mixing of solder and backside Au has been observed on the front-side of wafers, as it had traveled through the backside vias. Not only does mixing adversely affect via resistance, it also forms brittle $AuSn_4$ intermetallic, causing spectacular failures. At assembly, die are picked and placed onto a solder pre-form on the substrate. The substrate is then reflowed to fuse the solder with the Au top layer of the solder metallization and form Ni_3Sn_4 at the NiV surface. In the case of our failed die, solder penetrated under the NiV layer and mixed with the backside Au during reflow. The solder penetration distance is dependent on the solder-attach process. There were two methods for solder attachment: solder wire and solder paste, each done at different assembly sites. Solder wire attach sustain reflow temperatures on the die for approximately four seconds and resulted in acceptable yields, despite having die edges exposed. Solder paste processes sustain reflow temperatures for greater than 20 seconds and caused 100% failures (Fig. 1). For this work, our only option was the assembly factory using solder paste. Without the option of alternative assembly factories, a fab process change was explored. Our goal was to develop a process compatible with solder paste assembly methods.

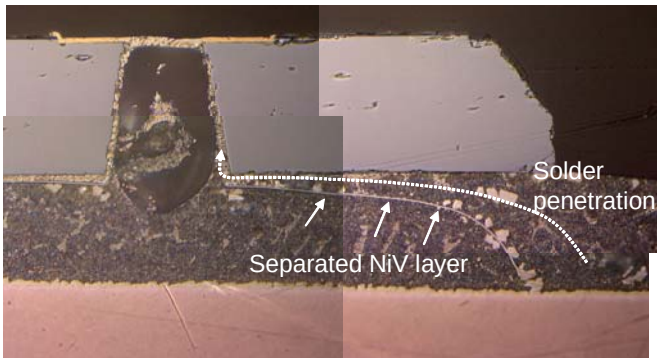

Figure 1 SEM Cross-sections of the failed die revealed solder mixed with backside Au layer underneath the solder metal stack using solder paste die attach.

EXPERIMENTAL

The solution required us to use existing equipment and process capabilities within Freescale Tempe Fab. We intended to create an "edge seal" since the solder mixing problem originated from the edge of the die created by the saw street. The edge of the die, specifically the edge of the backside Au, is not protected by the NiV solder barrier. The process steps used for initial evaluation began by creating "street" patterns in the backside Au using common photolithography and wet etches prior to solder metallization

(Figure 2). An important consideration was making the Au street wide enough to prevent the saw process from cutting through what will eventually be the edge seal. To protect the newly formed sidewall of the backside Au (created by the formation of a street) from solder mixing, solder metallization must cover its edge. Solder metallization consists of a Ti adhesion layer, followed by NiV solder barrier, and finally, Au. These particular devices also contained through-wafer backside vias. An additional layer of Ti is patterned inside the backside vias for solder repulsion during reflow. Figure 3 represents all layers on the backside of the wafer with respect to through-substrate vias. Figure 4 is a scanning electron microscope (SEM) image of an actual die edge with the edge seal process. It should be noted that processing is performed after wafer has been thinned and mounted to a support substrate.

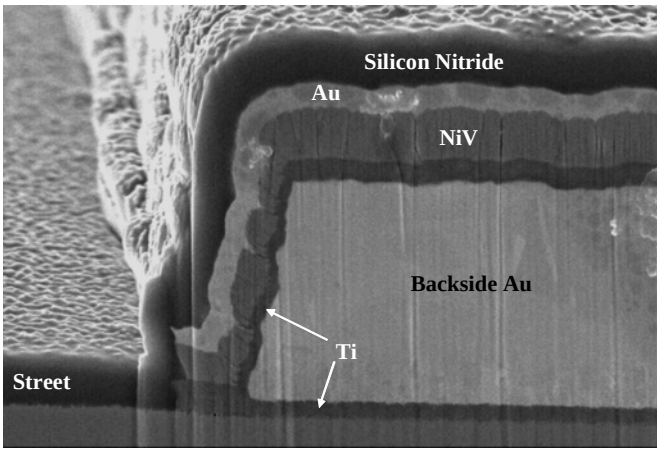

Figure 4 Die edge with edge seal process. Note that the edge of the backside Au is protected from PbSn solder penetration. Silicon Nitride deposited for sample preparation.

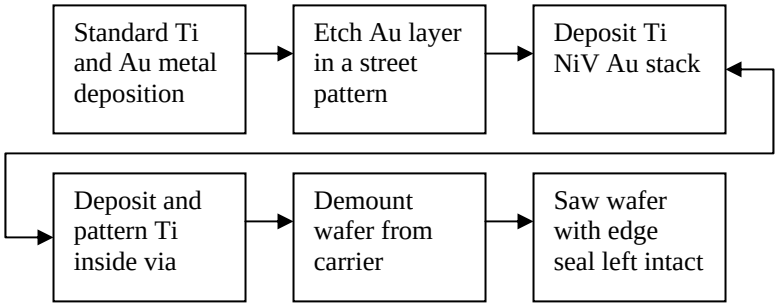

Figure 2 Block diagram of edge seal processing steps.

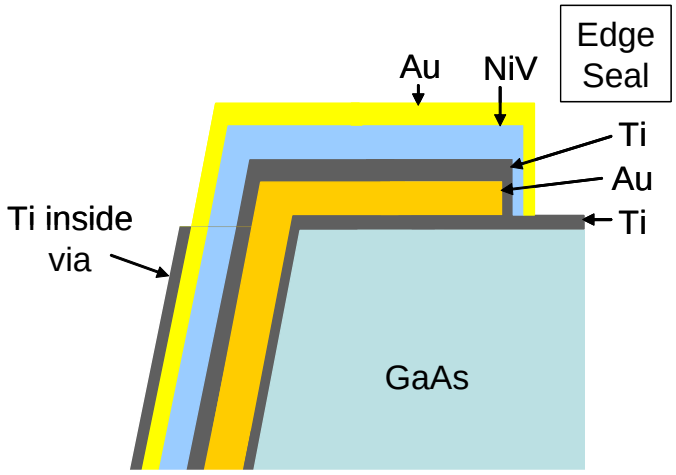

Figure 3 Completed backside metallization from the GaAs substrate: thin Ti adhesion layer, thick Au ground plane, thin Ti adhesion layer, NiV solder barrier and bonding surface, Au to cap NiV from oxidation and for solder bonding, and Ti back-via liner. (Not to scale)

RESULTS

Die were assembled using a solder paste process and evaluated for both solder voids and solder mixing at die edge. Solder voids were observed by x-ray imaging (Fig. 5) and corresponded to backside vias. The total die area contact was acceptable. Following assembly testing, optical microscopy revealed that the edge seal had prevented penetration of PbSn solder from mixing with backside Au (Fig 6). From approximately 200 die assembly tested, die using solder paste that had the edge seal process matched that for non-edge seal die using solder wire assembly (acceptable yields). Die tested without edge seal using solder paste assembly yielded zero.

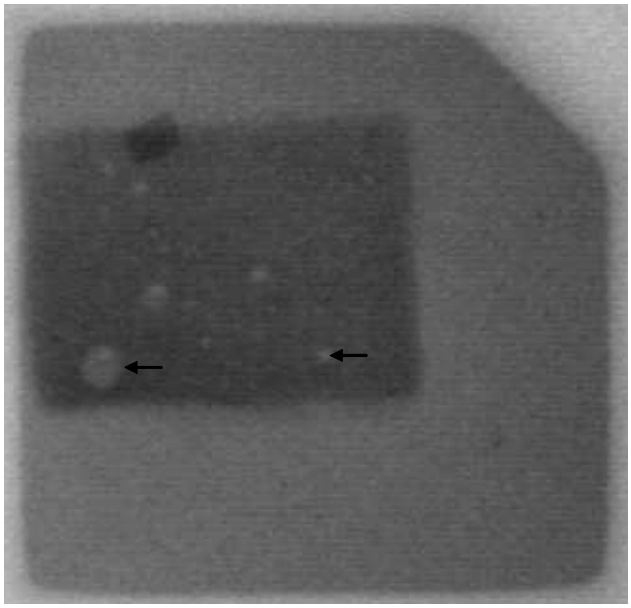

Figure 5 X-ray image of die with edge seal process following solder paste assembly. Arrows indicate solder voids that corresponded to backside (through-substrate) vias.

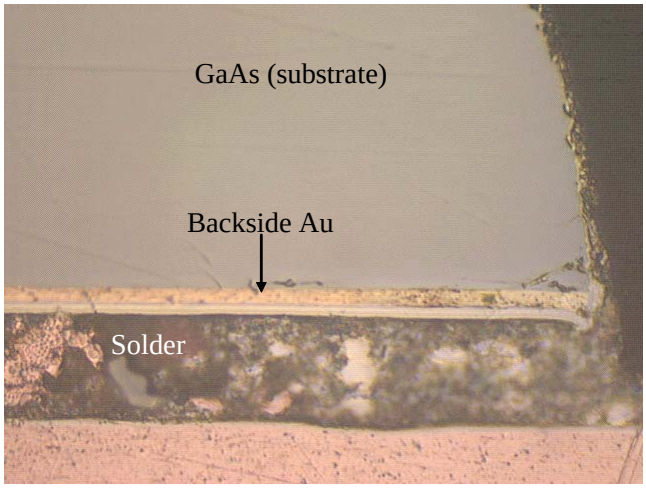

Figure 6 Optical image of die with edge seal process following solder paste assembly. Note that the backside Au (arrow) remains isolated from PbSn solder.

CONCLUSION

The edge seal process corrected the assembly failure. Based on these results, a viable method has been developed for devices requiring a solder paste process. In addition, the use of this process can be extended to use with solder wire process where solder mixing with Au is also a known, but less problematic issue.

ACKNOWLEDGEMENTS

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ACRONYMS

PHEMT: Psuedomorphic High Electron Mobility Transistor
SEM: Scanning Electron Microscope