

# Status of SiC Power Devices and Manufacturing Issues

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## Abstract

SiC materials and device technology has entered a new era with the commercialization and acceptance of 600 V/10 A and 1200 V/10 A Schottky Barrier Diodes (SBDs) in the marketplace. These diodes are finding applications in the Power Factor Correction (PFC) stage of Switch Mode Power Supplies (SMPS). SiC power MOSFETs with ratings of 800-1200 V up to 10 A will soon be commercially available. The next step is to integrate the SiC MOSFET and Schottky diodes in a power module for PFC and motor control applications. The motor control application requires 1200 V/100 A devices. This represents a factor of 10 increase in the die area and hence the new manufacturing challenges have to be met in order to maintain high yields. These challenges include reduction of defects on the 3" wafers during epitaxy, flatter wafers and better control on the manufacturing processes such as guard ring dimensions. The other manufacturing issues are threshold voltage control in power MOSFETs, use of high temperature implants and bigger diameter substrates (4 inch in near future and 6 inch in a few years).

## INTRODUCTION

SiC power devices are beginning to be commercialized. The 300 V, 600 V and 1200 V SiC Schottky diodes with current ratings in the range of 1 - 10 A were released for production in 2001. Today, there are more than 3 million parts installed in switch mode power supplies. The main benefit of the SiC Schottky diode is almost complete elimination of the reverse recovery charge which is present in the conventional Si fast recovery PiN diodes. The absence of the reverse recovery charge allows the designer to remove snubber circuits and reduce the number of active switches in the Power Factor Correction (PFC) circuit without any increase in switching frequency (80-100 kHz) leading to higher efficiency (efficiency gain of 1-2% points) [1]. Alternatively, the gain in efficiency can be traded with higher switching frequency (200 - 300 kHz) which results in a much smaller circuit due to the reduction in the size of the EMI filter and the boost inductor [2].

The next step is to manufacture a SiC 800 V/1-10 A MOSFET for replacement of Si MOSFET in the PFC circuit. This would lead to a further efficiency improvement of 1-2% points. The combination of SiC Schottky diodes and MOSFETs can achieve an efficiency improvement of 2-

4% at standard switching frequencies or 60-70% reduction in size at the same efficiency but a higher switching frequency of 500 kHz to 1 MHz.

The other major application of SiC MOSFETs and Schottky diodes is in motor control. In a typical three phase pulse width modulated (PWM) inverter system, there are six switches (silicon IGBTs) with six free wheeling diodes (Silicon PiN diodes). When these components are replaced with SiC MOSFETs and Schottky Diodes, there is an approximately a 80% reduction in total losses (switching + conduction losses) [3]. This is expected to result in an efficiency improvement of about 4-6% points. In addition, cooling requirements are substantially reduced in direct proportion to the reduction in losses. However, this application requires 1200 V/100 A devices - a factor of 10 increase in the die area. This represents unique challenges for manufacturing such as reduction of defects in the substrate and epilayers, flatter wafers, better control on the manufacturing processes such as guard ring dimensions and an increase in substrate diameter from the current 3" to possibly 6" to bring the manufacturing cost down.

## SiC JUNCTION BARRIER SCHOTTKY (JBS) DIODES

Figure 1 illustrates the construction of the SiC Junction Barrier Schottky (JBS) diode. It consists of an ion-implanted  $p^+$  grid in the active area and an edge termination. The structure shown in Fig. 1 employs a Junction Termination Extension (JTE) termination structure, which can be replaced with a multiple floating guard rings (FGRs) structure. The advantage of the FGRs over JTE is that the FGRs can be implanted along with the JBS grid thus reducing one mask step. The function of epilayer-1 is to prevent the high electric field from reaching the substrate. The epilayer-2 is designed to block a given breakdown voltage. The backside ohmic contact is formed by sputtering a thin Ni layer and annealing it at 1000°C for a few minutes in Ar ambient. The Schottky metal can be either Ni, Pt or Ti depending upon the desired temperature of operation. For operating temperatures below 200°C, Ti is the preferred Schottky metal because of its lower barrier height. For high temperature operations, higher barrier height metal, such as

Ni or Pt should be used. A thick Ag layer is deposited on the backside for die attach processes, and a thick Al layer is deposited on the top side for wire bonding.

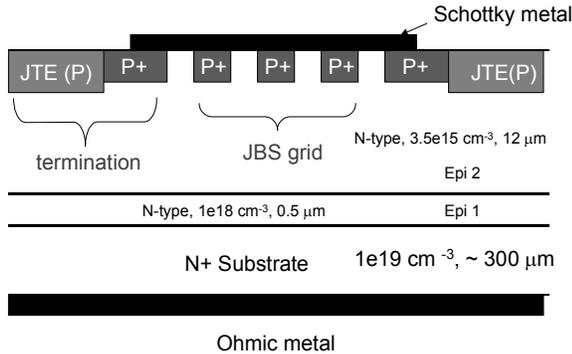


Fig. 1. Cross-section of the 1200 V SiC JBS Diode showing the edge termination and the P<sup>+</sup> JBS grid.

300 V (10A and 20A), 600 V (1A, 4A, 6A, 10A, and 20A) and 1200 V (5A, 10A, and 20A) Schottky diodes are commercially available [4]. These devices have relatively small current ratings, and the applications of these devices are limited to switch mode power supplies (SMPS). For motor control applications, such as hybrid vehicles, devices with high current ratings are required. Continuous efforts were made to scale up the diodes. 4H-SiC JBS diodes with ratings of 1200 V, 75 A have been successfully demonstrated [5]. Fig. 2 shows a photograph of the 1200 V, 75 A JBS diodes fabricated on a 3 inch 4H-SiC wafer. The chip size of the device is approximately 6 mm x 8 mm. Fig. 3 shows the forward I-V characteristics of the diode at room temperature, measured with Tektronix 371 curve tracer. A forward current of 75 A, which corresponds to a current density of 180 A/cm<sup>2</sup>, was measured at a forward voltage drop of 1.75 V. Fig. 4 also shows the reverse I-V characteristics of the diode. At a reverse voltage of 1270 V, a leakage current of 123 μA, which corresponds to 0.25 mA/cm<sup>2</sup>, was measured at room temperature.

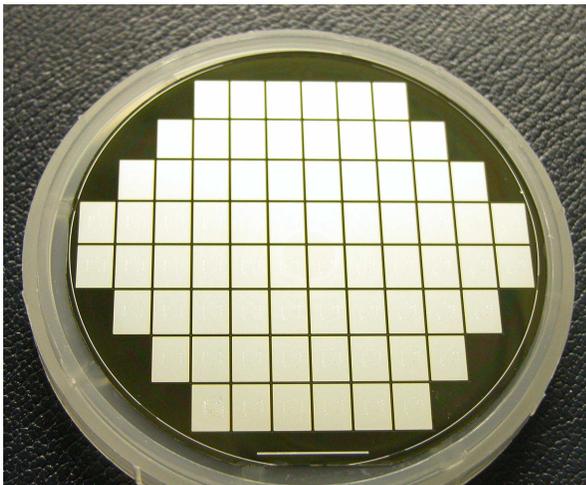


Fig. 2. 1200 V, 75 A 4H-SiC JBS diodes fabricated on a 3 inch wafer.

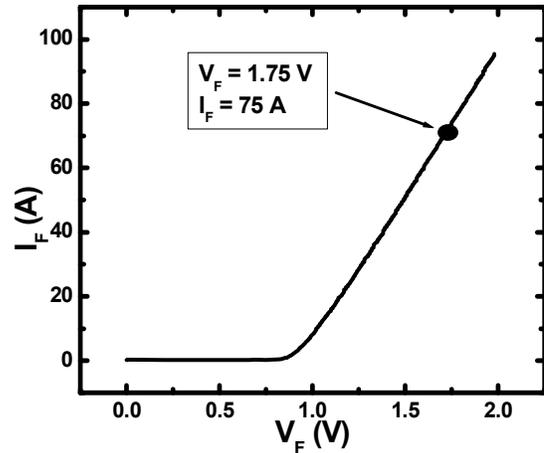


Fig. 3. Forward I-V characteristics of a 6 mm x 8 mm 4H-SiC JBS diode.

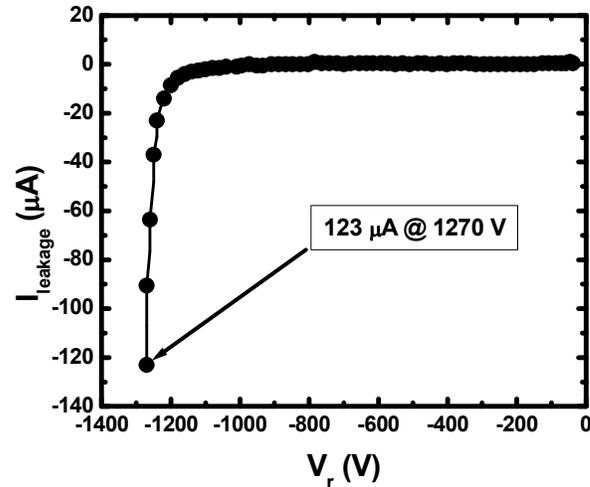


Fig. 4. Reverse I-V characteristics of a 6 mm x 8 mm 4H-SiC JBS diode.

Low breakdown voltage of the devices has been typically the principal reason for loss in yield. So far, the most dominant yield limiters are various types of material defects, which include micropipes, screw dislocations, and edge dislocations [6]. Micropipe density has been decreasing steadily over the past few years and are no longer the most dominant material defect [7]. However, dislocation density is still in the order of 1000/cm<sup>2</sup>, and further reduction is needed for higher device yield.

Edge termination structure also plays an important role in the breakdown yield. Fig. 5 shows an image of a 4H-SiC JBS diode in blocking state, captured using a high sensitivity CCD camera. This device is terminated with floating guard ring structure. The floating guard ring structure provides cost effective edge protection because it can be formed at the same time with the p<sup>+</sup> JBS grid. However, for stable high voltage operations, a more robust edge termination structure is desired. In Fig. 5, a very localized avalanche (See area surrounded by rectangle) was observed, which indicates that

the performance of the floating guard ring structure was not adequate. Use of multiple JTE can provide a more tolerant, better performing edge termination structure [8]. However, implementation of multi-zone JTE structure in SiC requires multiple ion implantations, due to lack of impurity diffusion in SiC, and can be very costly. An optimal compromise must be made between fabrication cost and device performance for successful commercialization of SiC JBS diodes.

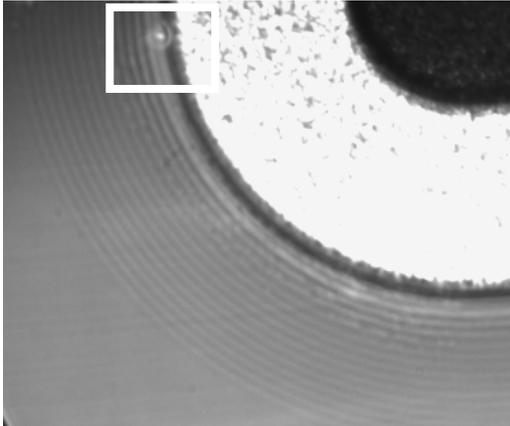


Fig. 5. Image of a 4H-SiC JBS diode with floating guard ring edge termination in blocking state. A localized avalanche can be observed in the termination area (See inside rectangle). The image was taken using a high sensitivity CCD camera.

#### SiC MOSFETs

The 4H-SiC DMOSFET structure is shown in Fig. 6. The MOS channel length is defined by the p-well and n<sup>+</sup> implants, and can range from 0.5 μm to 1.5 μm. Electrons flow laterally from the n<sup>+</sup> source, through an inversion layer across the implanted p-well, then flow vertically through the JFET region formed by two adjacent p-well regions, and then through the lightly doped n<sup>-</sup> drift region into the drain. The blocking voltage of the MOSFET is determined by the doping concentration of the n<sup>-</sup> epilayer. For 1200 V devices, an epilayer with a doping concentration of 6x10<sup>15</sup> cm<sup>-3</sup> and a thickness of 12 μm can be used. A thermally grown oxide layer is typically used as gate dielectric due to its repeatability and stability. Typically, the gate oxide is nitrided in NO or N<sub>2</sub>O to reduce MOS interface state density, which improves the transconductance of the MOSFET.

Figure 7 shows the on-state I-V characteristics of a 1.8 kV 4H-SiC DMOSFET. The device has a 500 Å thick gate oxide. The gate oxide electric field was limited to approximately 3 MV/cm (V<sub>gs</sub> = 15 V). The active area of this device is 0.0936 cm<sup>2</sup>. An on-resistance of 85 mΩ (R<sub>on,sp</sub> = 8 mΩ-cm<sup>2</sup>), and a drain current of 50 A ( 534 A/cm<sup>2</sup>) at a forward drop of 5.7 V were measured at room temperature. At an operating temperature of 150°C, the on-resistance increases to 100 mΩ (9.4 mΩ-cm<sup>2</sup>). A slight negative shift in MOS threshold voltage at elevated temperatures decreases

the MOS channel resistance at a fixed gate bias. This cancels out, to some extent, the increase in drift layer resistance, resulting in temperature stable on-resistance.

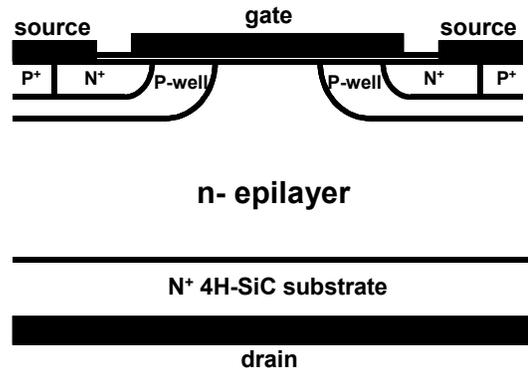


Fig. 6. Simplified cross-section of the SiC DMOSFET.

Figure 8 shows the blocking characteristics of the 4H-SiC DMOSFET, measured on-wafer using a Tektronix 371A curve tracer. The device was covered in Fluorinert oil to prevent arcing in air. The device is normally off, and showed stable avalanche characteristics at a V<sub>DS</sub> of 1.8 kV with a V<sub>GS</sub> of 0 V. The ideal parallel plate peak electric field for the drift epilayer used in this device is 2.15 MV/cm.

The biggest challenge in commercialization of the 4H-SiC MOSFET is control of the threshold voltage. The room temperature threshold voltage is approximately 3.5 V, which decreases to 2.2 V at 150°C. However, for power switches, the drain current should be less than 1 μA in off-state. It is shown in Fig. 9 that the gate bias should be less than 1.55 V at room temperature and 1.05 V at 150°C to keep the device at off-state. The low current threshold voltage of this device is very close to zero. It should be noted that the noise margin of this device is extremely small – a small glitch in the gate drive can turn the device on. In addition, the device can have a negative threshold voltage with a very slight variation in fabrication process. This is detrimental for power switching applications. A positive shift of threshold voltage is needed for more stable operations and for ensuring a normally-off behavior.

#### CONCLUSIONS

In summary, the manufacturing of SiC Schottky diodes has been on-going for more than four years. It initially began in 2001 on 2" 4H-SiC wafers, subsequently moved to 3" wafers and is now poised to move to 4" wafers. During this time, defects in the substrate and epilayers have been identified as the principal reason for loss in yield. SiC MOSFETs are ready for full-scale production and would probably be introduced sometime in 2006. The threshold voltage control is the single biggest challenge which is caused by very high fixed positive charge in the gate oxide layer.

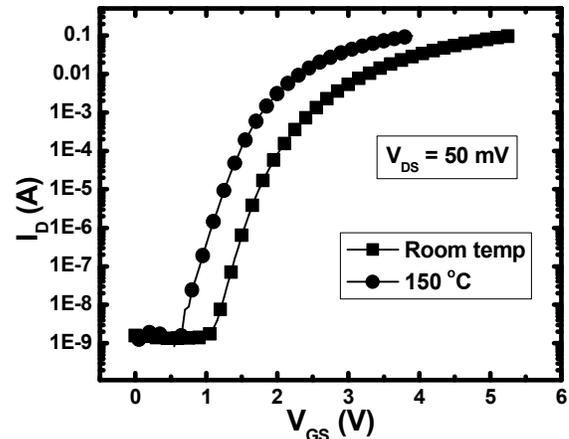
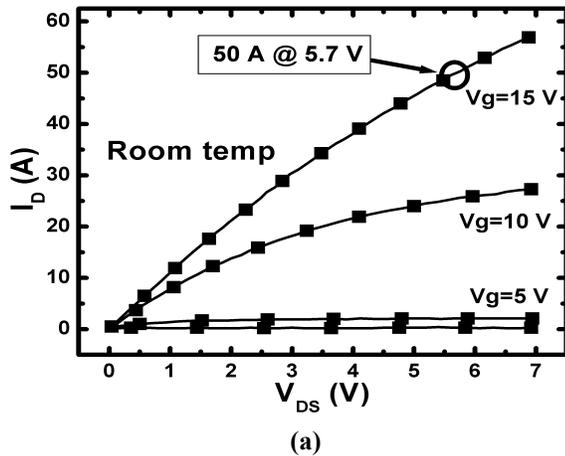


Fig. 9. Subthreshold behavior of a 0.0936 cm<sup>2</sup> 4H-SiC DMOSFET.

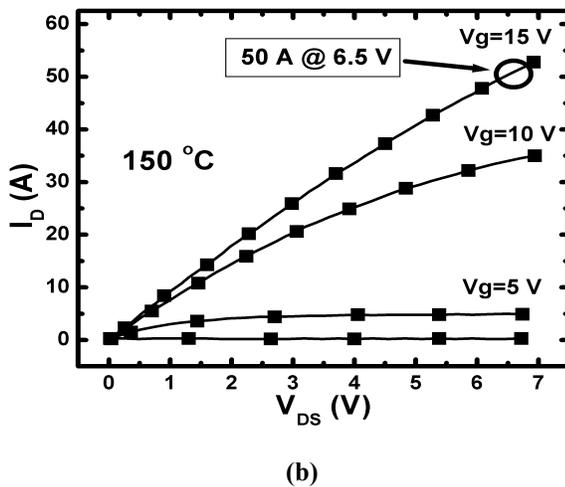


Fig. 7. On-state characteristics of a 0.0936 cm<sup>2</sup> 4H-SiC DMOSFET. (a) at room temperature, and (b) at 150°C.

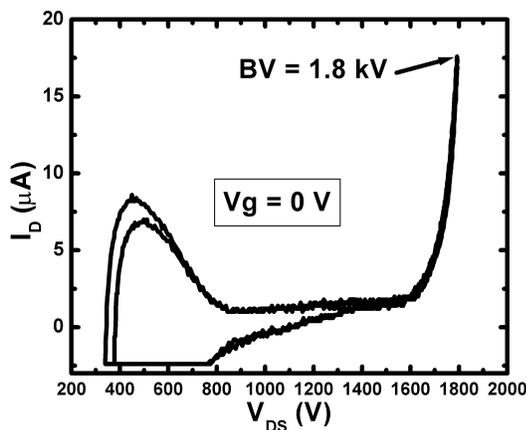


Fig. 8. Blocking characteristics of a 0.0936 cm<sup>2</sup> 4H-SiC DMOSFET at room temperature.

#### ACKNOWLEDGEMENTS

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