Low Power High-Speed Circuits with InAs-based HBT Technology

C. Monier, A. Cavus, R.S. Sandhu, A. Oshiro,
D. Li, E. Kaneshiro, D. Matheson, B. Chan, and A. Gutierrez-Aitken

Northrop Grumman Space Technology, Redondo Beach, CA 90278
e-mail: cedric.monier@ngc.com, Tel: (310) 812-6129

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Abstract

High indium content $In_{0.86}Al_{0.14}As/In_{0.86}Ga_{0.14}As$ double heterojunction bipolar transistors (DHBTs) were grown on InP substrates using thin 6.0 Å metamorphic compositionally graded buffer layers. Good DC and RF characteristics have been demonstrated, with high gain (~30), breakdown voltage greater than 2.5 V, turn-on voltage reduction by a factor of two compared to existing InP bipolar technology, peak frequencies f_T and f_{MAX} exceeding 150 GHz (measured at low current without applying any voltage at the base-collector junction). Fully functional circuits with complexity ranging from 20 to 1100 transistors have been successfully demonstrated on thin 6.0 Å metamorphic buffers, with power dissipation reduced by a factor of 2 compared to equivalent circuits designed with InP.

INTRODUCTION

The $In_xGa_{1-x}As$ system with high indium content x > 80% has several unique advantages over InP and GaAs such high electron mobility and large peak saturation velocity for extending the performance of electronic devices to high frequency at reduced power consumption. In bipolar logic circuits, the use of high indium content materials with energy band gap less than 0.5 eV in the base layer of an HBT can potentially reduce by 50% the device turn-on voltage V_{BE} compared to conventional III-V technologies. That will directly translate to lower supply voltage and be used as alternatives to InP-based HBTs for low power circuit applications. This paper summarizes the current status of NGST's narrow band gap HBT technology using a 6.0 Å metamorphic approach, with highlights on device characteristics, process integration and low power circuit results based on material systems with lattice parameter towards that of InAs.

METAMORPHIC APPROACH

Among traditional challenges related to narrow-band-gap materials is the lack of a semi-insulating substrate around 6.05 Å lattice parameter [1-3]. Our approach consists of using a metamorphic platform grown on semi-insulating InP wafers using solid-source MBE [4]. An $In_xAl_{1-x}As$ strain-relieved buffer layer is graded from x = 0.52 towards InAs (x=1) to obtain lattice constants that are not presently available. InAlAs is chosen over InGaAs because of its larger thermal conductivity. This approach offers the possibility of using any lattice parameter between InP and InAs for innovative narrow band gap HBT band gap engineering.

The high density of threading dislocations and crosshatch pattern typically observed with metamorphic wafers can severely impact the manufacturing of integrated circuits. Graded buffer layer (GBL) characteristics have been optimized in terms of total thickness, dislocation density and surface roughness. Growth optimization enables high indium content 6.0 Å $In_{0.86}Al_{0.14}As$-terminated metamorphic graded buffer layers with minimum surface roughness (RMS < 5 nm), total buffer thickness less than 1 micron, and density of dislocations in the vicinity of 10^6 cm^{-2}, to serve as virtual substrate for narrow band gap HBTs.

Cap $In_{0.86}Ga_{0.14}As$ – 1000 Å (2e19 cm^{-3})
Emitter $In_{0.86}Al_{0.14}As$ – 1000 Å (5e17 cm^{-3})
Base $In_{0.86}Ga_{0.14}As$ - 400 Å (3e19 cm^{-3})
Collector $In_{0.86}Al_{0.14}As$ -2500 Å (4e16 cm^{-3})
Sub-Collector $In_{0.86}Al_{0.14}As$ – 4000 Å (1e19 cm^{-3})
Buffer Graded $In_xAl_{1-x}As$ (from 52 to 86 %)
Substrate SI InP

Figure 1 Schematic of the narrow-band-gap 6.0 Å $In_{0.86}Al_{0.14}As/In_{0.86}Ga_{0.14}As$ double- HBT structure.

TRANSISTOR DESIGN AND FABRICATION

The total thickness of the baseline GBL is less than 1 micron. All active layers grown on top of the metamorphic buffer are lattice-matched to the final In buffer composition. The Double Heterojunction Bipolar Transistors (DHBT) device structure is based on the 6.0 Å $In_xAl_{1-x}As/In_xGa_{1-x}As$ material system using 86 % indium. This system provides significant low operating voltage with an energy band gap in the $In_{0.86}Ga_{0.14}As$ base of 0.45 eV, which is 40% below the energy band gap of $In_{0.53}Ga_{0.47}As$ used in lattice-matched InP HBTs. $In_{0.86}Al_{0.14}As$ used for collector and emitter layers, offers larger bandgap than InAsP for more favorable heterojunction band alignment and improved breakdown properties.

Figure 1 describes the 6.0 Å DHBT epitaxial structure. The compositionally graded $In_{0.86}Ga_{0.14}As$ base layer thickness is 400 Å, with $3x10^{19}$ cm^{-3} Be doping concentration and is followed by a linearly-graded base-emitter interface. The Indium-rich emitter structure will ensure low emitter resistance. The DHBT design, with the use of 2500 Å $In_{0.86}Al_{0.14}As$ collector layer is particularly desired to improve breakdown voltage, which is naturally low for narrow-band-gap materials.

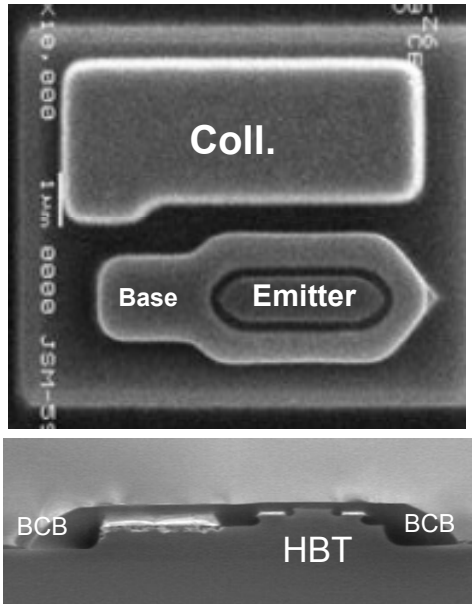


Figure 2 Top view and cross-section SEM pictures a 6.0 Å HBT with 0.8 um emitter width.

Small area 6.0 Å devices have been fabricated using most of the NGST standard InP HBT front side and back side processes with some minor process changes [5, 6]. In order to take full advantage of this narrow band gap transistor technology for low power applications, the emitter active area needs to be laterally scaled towards sub-micron dimensions. A 6.0 Å HBT i-line stepper projection lithography process with emitter width of 0.8 and 0.6 µm has been developed, as shown in Figure 2. To achieve good isolation between metamorphic transistors, the isolation etch is extended into the InAlAs GBL, resulting in a much taller isolation mesa compared to traditional InP technology. Another difference with our InP HBT production process is the use of bizbenzocyclobutene (BCB) in replacement of conventional SiN dielectric for better passivation of 6.0 Å devices. The use of BCB to encapsulate the active devices necessitates an additional etch step to remove the dielectric elsewhere and have all passive elements directly on the substrate, including 20 and 100 Ω/□ NiCr thin-film resistors and MIM capacitors. Two layers of gold with airbridge crossovers are used for circuit interconnect. A robust high-yield 3mil backside process including thinning, dry-etched vias, and plated backside gold completes the circuit fabrication.

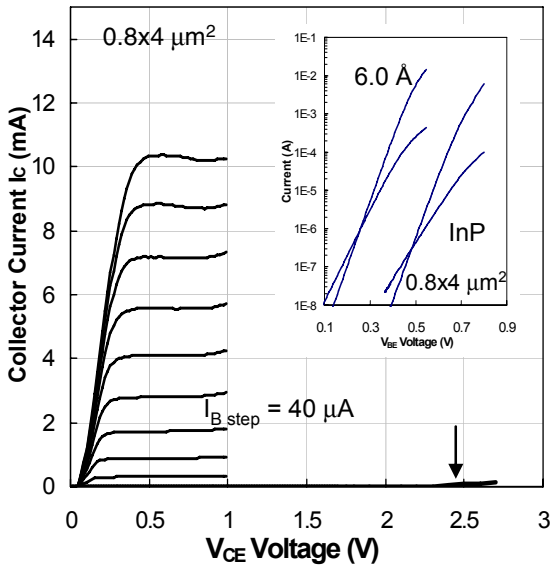
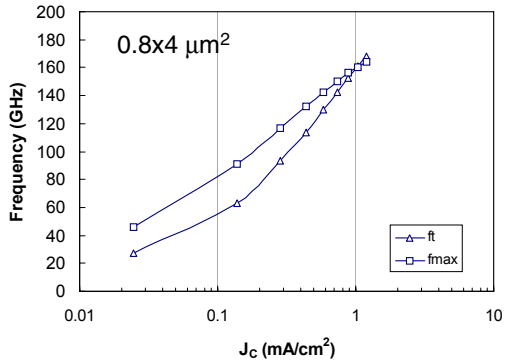


Figure 3 Common-Emitter I-V measurements from a 6.0 Å $In_{0.86}Al_{0.14}As/In_{0.86}Ga_{0.14}As$ HBT The inset compares gummel plots from InP and 6.0 Å HBTs of identical emitter size (A_E = 0.8x4 µm²).

6.0 Å HBT DC and RF Characteristics

The inset in Figure 3 compares Gummel plots of DHBTs from InP and 6.0 Å technologies of identical emitter area (0.8x4 μm^2). This clearly shows that the turn-on voltage (the base emitter voltage needed to achieve a certain amount of output current) is reduced by almost half with the use of a narrow-band-gap approach compared to InP. The 6.0 Å device exhibits a DC gain β near 30. Reverse collector-base leakages around 10 nA are typically observed in the range of operating bias intended for this low-power technology. Figure 3 also displays the common-emitter IV characteristics of a 6.0 Å DHBT. No current blocking is observed up to 3 $mA/\mu m^2$. Despite the narrow-band-gap collector, off-state breakdown voltages BV_{CE0} exceeding 2.5 V are measured. A 30 % reduction of the knee voltage is observed compared to InP-based HBTs of equivalent size, particularly advantageous for high power-added efficiency applications at low power.

Peak frequencies f_T and f_{MAX} exceeding 150 GHz (shown in Figure 4 for A_E = 0.8x4 μm^2) have been measured at low current without applying any voltage at the base-collector junction (V_{CE} = V_{BE} ~ 0.5 V). Improvement on the maximum oscillation frequency f_{MAX} has been made possible with more p-type dopants incorporated (up to $3x10^{19}$ cm^{-3}) for lower base sheet resistance. Table 1 summarizes RF characteristics for 6.0 Å DHBTs of various sizes, with comparable performance to the production InP HBT technology but achieved at lower operating voltages.



Size (um²)	f_T (GHz)	f_{max} (GHz)	V_{CE} (V)	I_C (mA)
0.6x2	170	155	0.5	1.3
0.6x4	170	170	0.49	2.6
0.6x6	145	140	0.48	3.8
0.8x2	185	160	0.51	1.8
0.8x4	165	165	0.49	3.7

Figure 4 Extrapolated small-signal unity current gain f_T and unity power gain f_{MAX} for a 6.0 Å $In_{0.86}Al_{0.14}As/In_{0.86}Ga_{0.14}As$ DHBT with A_E = 0.8x4 µm². The table summarizes RF characteristics from the 6.0Å sub-micron HBT technology.

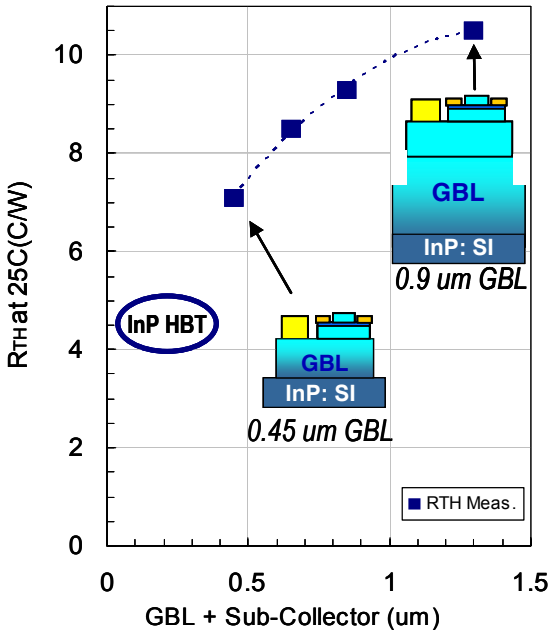


Figure 5 Measured thermal resistance R_{TH} from 6.0 Å DHBTs as a function of versus total $In_xAl_{1-x}As$ thickness (from metamorphic buffer and sub-collector).

THERMAL RESISTANCE IMPROVEMENT

Metamorphic buffers using ternary materials have much higher thermal resistance (R_{TH}) than binary components (InP). This large R_{TH} will increase the device junction temperature with severe consequences on device reliability. Recent effort has been focused on reducing the buffer thickness for minimized device R_{TH} [7]. The 6.0 Å DHBT has been grown on top of various GBL thickness (from 0.9 µm down to 0.45 µm) in order to identify the minimum thickness that can be used for better thermal conduction while keeping the same device properties, at no DC/RF/yield characteristic expenses. XTEM and EPD analysis shows that comparable material quality (same level of dislocations, surface roughness) can be achieved with thinner GBLs. This is confirmed by electrical characteristics on small area devices showing no DC or RF difference (same gain, turn-on, leakage level, peak frequencies) between thick-0.9 µm and thin-0.45 µm.

Figure 5 shows that the measured R_{TH} scales well with the ternary InAlAs thickness. A significant improvement by 35% in thermal conduction is realized with the thin buffer compared to the baseline thick buffer design. This is still higher than InP HBT thermal resistances but this decrease corresponds to a junction temperature reduction of 20 °C, for significant impact on reliability performance.

METAMORPHIC 6.0 Å HBT-BASED CIRCUIT RESULTS

6.0 Å HBT device library and models have been developed to design low power high speed digital and mixed circuit applications. Table 1 lists all circuits that have been fabricated on 6.0 Å metamorphic buffers to assess the manufacturability level of this novel technology.

TABLE 1 List of demonstrated circuits based on 6.0 Å metamorphic HBT technology.

6.0 Å HBT Circuits	Transistor Count	Measured Circuit Characteristics
Equalizers	20 HBTs	35 Gbps max. operation
Div-x-2	60 HBTs	1 mW / latch at 12 GHz 2.5 mW / latch at 22 GHz 5.5 mW / latch at 35 GHz Max. frequency of 47 GHz
Div-x-4	130 HBTs	DC-46 GHz
Delay Chain	250 HBTs	11 ps Delay per stage
1:6 DEMUX	630 HBTs	3 GHz fclock. Pdc = 500 mW
6:1 MUX	750 HBTs	3 GHz fclock. Pdc = 600 mW
4-bit ADC	1100 HBTs	1.3 GHz Clock. Pdc = 600 mW

Figure 6 shows the measured output signal of a divide-by-2 circuit with a maximum clock frequency of 47 GHz, using 0.8x4 µm² devices in the divider flip-flop. This generic digital building block circuit contains about 60 transistors. Functional yield comparable to what observed with InP has been

demonstrated. Ultra low power-per-latch values have also been measured by scaling the emitter area down to 2 μm^2.

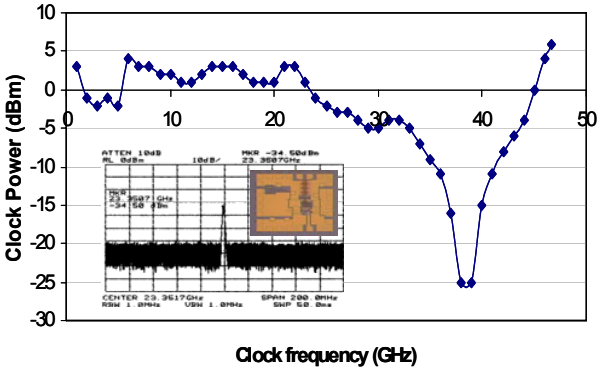


Figure 6 Output spectrum and sensitivity plot of a divide-by-2 circuit using 6.0 Å narrow-band-gap HBTs (die photo shown in the inset) with maximum input clock frequency of 47 GHz.

A 4-bit flash Analog-to-Digital Converter (ADC) circuit has been designed with 1100 HBTs (typical device size of 0.8x4 um^2). The die size is 3.2 mm x 3.2 mm (picture shown in Figure 7). This 4-bit ADC uses a flash implementation to convert its analog input into 4 bits. The analog input is set at 4 MHz using differential CML levels. The clock input is run at 800 MHz with differential CML. The path of the analog data goes through an analog resistor spreader ladder, pre-amplifiers, comparators, thermometer to binary weight ROM decode logic. Typical measured output waveform is shown in Figure 7. The chip dissipates 40% less power than an equivalent circuit based on InP HBTs, primarily due to lower input voltage. This is the largest narrow band gap circuit demonstrated by NGST using that technology and among one of the most complex III-V metamorphic chips. Note that the majority of the circuits presented in this paper were fabricated on both thick 0.9 um and thin 0.45 µm metamorphic GBLs and show equivalent RF and yield performance.

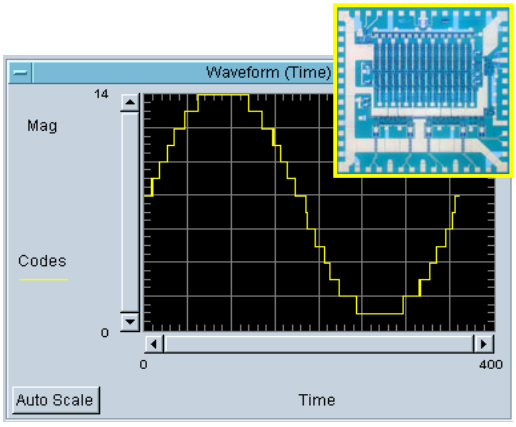


Figure 7 Measured output of 6.0 Å HBT 4-bit ADC circuit. This mixed-signal circuit with 1100 HBTs dissipates ½ the power compared to an equivalent circuit based on InP HBTs.

ACRONYMS

DHBT: Double Hetero-junction Bipolar Transistor
BCB: bizbenzocyclobutene
GBL: graded buffer layer

CONCLUSIONS

High indium content $In_xAl_{1-x}As/In_xGa_{1-x}As$ single and double heterojunction bipolar transistors with 86% indium have been fabricated on InP semi-insulating substrates using a metamorphic approach. Device scaling and thermal management has been improved. Excellent DC and RF performance have been measured at very low operating voltages. Digital and mixed-signal circuits with complexity ranging from 20 to over 1000 HBTs have been successfully demonstrated, showing the potential this narrow band gap technology has for reducing power consumption in future high-speed applications.

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