Temperature Dependence of InGaP/InGaAs/GaAs pHEMTs

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Abstract

The temperature dependence of InGaP/InGaAs/GaAs pseudomorphic high electron mobility transistors (pHEMTs) has been characterized by current-voltage (I-V) and capacitance-voltage (C-V) methods from -60 °C to 80 °C. The threshold voltage and transconductance are found to decrease with temperature, while the source access resistance shows a modest increase with temperature. The threshold voltage and transconductance effects can be explained by the combined effects of a decreased effective Schottky barrier height due to barrier inhomogeneity and increased channel carrier concentration with increasing temperature, while the access resistance temperature dependence arises from opposing trends in carrier concentration and channel mobility.

Keywords: InGaP, GaInP, pHEMT, Schottky barrier, temperature dependence

INTRODUCTION

High-performance devices suitable for operation over wide temperature ranges are needed for many applications, including automotive, aircraft, and space technology [1]. Due to the chemical stability and large bandgap of InGaP lattice-matched to GaAs, pHEMTs based on InGaP appear to be a promising choice for these demanding uses. Their temperature-dependent performance, especially at high temperature, has become an important issue in state-of-the-art MMIC designs [2]. Although reports detailing the temperature-dependent characteristics of specific InGaP-based pHEMT designs have been published [2-3], little work regarding the physical mechanisms governing this dependence has been reported. In this paper, the temperature-dependent performance of 1-μm gate length InGaP/InGaAs/GaAs pHEMTs is examined and the underlying physical mechanisms are analyzed. This analysis provides insight into the physical basis for the observed pHEMT performance, which can guide the design of pHEMTs for extended temperature operation.

DEVICE FABRICATION

The InGaP-based pHEMT heterostructure was grown on semi-insulating GaAs substrates by metal-organic chemical vapor deposition (MOCVD). A 500 nm undoped GaAs buffer layer was first grown on the substrate and followed by a 10 nm undoped $In_{0.2}Ga_{0.8}As$ pseudomorphic channel layer, a 5 nm undoped $In_{0.49}Ga_{0.51}P$ spacer layer, a 15 nm Si-doped $In_{0.49}Ga_{0.51}P$ donor layer with doping level of 2.6×10^{18} /cm^3, a 10 nm undoped $In_{0.49}Ga_{0.51}P$ Schottky barrier layer, and a 40 nm Si-doped GaAs cap layer with doping level of 4×10^{18} /cm^3. The structure has a measured room-temperature mobility of 4110 cm^2/Vs and a sheet carrier concentration of 1.95×10^{12} /cm^2.

A schematic cross-section of the device structure is shown in Fig. 1. Device fabrication included wet chemical mesa isolation etching, with AuGe/Ni/Au source and drain ohmic contacts formed by conventional lithography, thermal evaporation, lift-off and rapid thermal annealing (RTA). The contact resistance obtained is 0.05–0.07 Ω-mm, as measured using TLM test structures. The gates were formed using selective gate recess wet etching, followed by electron beam evaporation and lift-off of Ti/Au metallization.

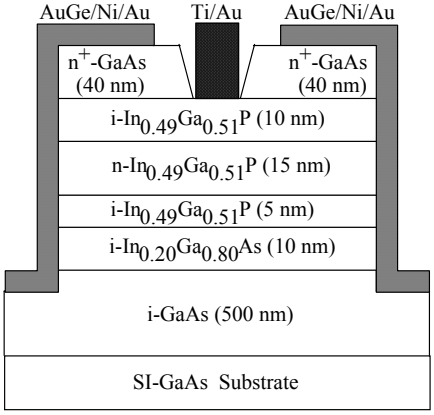

Figure 1. Schematic cross-sectional view of InGaP/InGaAs/GaAs pHEMT.

RESULTS AND DISCUSSION

The dc I-V characteristics and 1 MHz gate-to-source C-V characteristics of pHEMTs were measured on-wafer as a function of temperature from –60 °C to 80 °C. Room-temperature measurements before and after temperature cycling were identical in all cases, indicating that no bias or temperature stress effects were present. A typical I-V characteristic at room temperature is shown in Fig. 2. A peak extrinsic g_m of 274 mS/mm and a threshold voltage

(V_{th}) of –0.656 V were obtained. To investigate the intrinsic device performance, intrinsic g_m and V_{th} were extracted using $g_{m,\text{int}} = \frac{g_{m,ext}}{1 - R_s g_{m,ext}}$ [3] and $V_{g,\text{int}} = V_g - I_d R_s$, respectively. R_s is the source series resistance, and was extracted from measurements of TLM test structures as a function of temperature. The temperature dependence of the extracted source series resistance R_s, the calculated intrinsic transconductance, and the intrinsic threshold voltage are shown in Fig. 3. As shown in the inset of Fig. 3, R_s rises by approximately 40% with temperature from 0.89 Ω-mm at -60 °C to 1.25 Ω-mm at 80 °C.

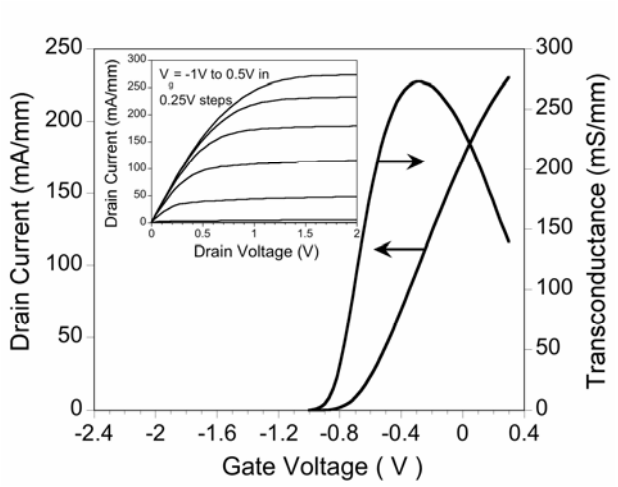

Figure 2. Drain current and transconductance as a function of gate voltage at room temperature. Inset is the common-source characteristic.

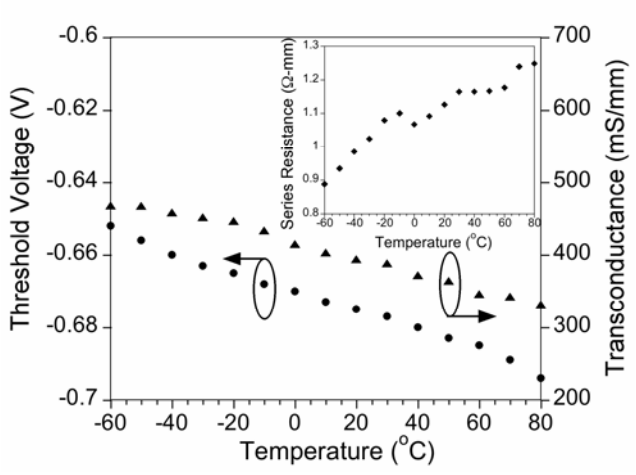

Figure 3. Intrinsic threshold voltage and transconductance as a function of temperature. Inset is the series resistance as a function of temperature extracted from TLM measurements.

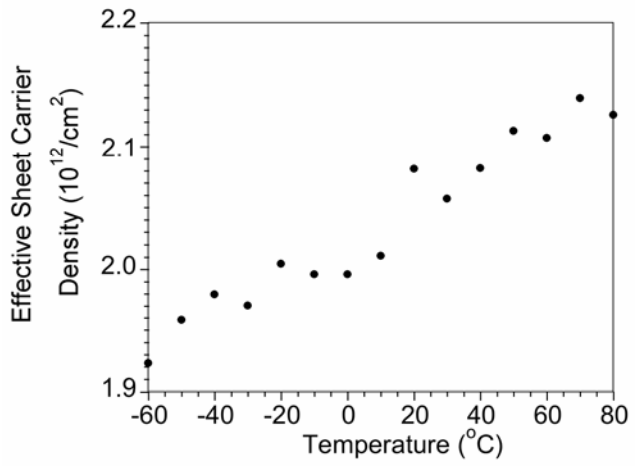

Figure 4. Effective sheet carrier concentration as a function of temperature extracted from C-V measurement.

Figure 4 shows the effective sheet carrier concentration, n_s, extracted from the measured gate-to-source C-V data. As shown in Fig. 4, n_s increases from 1.92×10^{12} /cm^2 to 2.13×10^{12} /cm^2, for an increase of 11% from -60 °C to 80 °C. Since R_s is inversely proportional to the carrier concentration-mobility product ($R_s \propto \frac{1}{n_s \mu_n}$), the observed 40% increase in R_s and 11% increase in n_s implies a 36% decrease in μ_n over temperature. For comparison, a $\mu_n \propto \frac{1}{T}$ dependence would result in a 40% drop in mobility over this temperature range. In addition, a power-law curve fit to the intrinsic transconductance and the effective sheet career concentration as a function of temperature gives $T^{-0.73}$ and $T^{0.20}$ dependencies, respectively. Because the transconductance of a pHEMT is expected to be proportional to both the electron concentration (n_s) and the saturation velocity (v_{sat}), v_{sat} should be expected to go as $g_{m,\text{int}}/n_s$. Based on the extracted intrinsic transconductance (Fig. 3) and carrier concentration (Fig. 4), the trend in v_{sat} is obtained to be proportional to $T^{-0.93}$, in good agreement with the data reported previously ($v_{sat} \sim T^{-1}$) [4], showing that transconductance and sheet carrier concentration measurements are consistent with expected trends.

To investigate the observed shift in threshold voltage with temperature, the Schottky barrier heights (Φ_B) of the gate contacts were extracted using three different methods, denoted as Φ_{BI}, Φ_{BF}, and Φ_{BC}, respectively, and shown in Fig. 5. Φ_{BI} is the barrier height found from forward-bias current-voltage measurements of pHEMT gate-source diodes using the modified Norde method [5]. Φ_{BI} at 30 °C is found to be 0.626 eV, which is in good agreement with the value reported in previous literature (Φ_{BI} = 0.621 eV for Ti/Au gate contact on InGaP at room temperature [6]). Φ_{BF} is the flat-band barrier height calculated from Φ_{BI} using Eq. 1 [7], which is the fundamental barrier height under flat band conditions:

$$\Phi_{BF} = n\Phi_{BI} - (n-1)\frac{kT}{q}\ln\frac{N_C}{N_D} \quad (1)$$

Φ_{BC} is the barrier height inferred from capacitive effects, and was extracted from reverse-bias C-V measurements of the pHEMT's gate-source diode using Eq. 2 [8]:

$$\Phi_{BC} = V_{\text{int}} + \frac{kT}{q} + \frac{kT}{q}\ln\frac{N_C}{N_D} \quad (2)$$

where N_D is approximated by the extracted effective channel sheet carrier concentration divided by the donor layer thickness, and V_{int} is determined from the intercept on the gate voltage axis of a plot of $1/C^2$ vs. gate voltage.

The gate Schottky barrier height extracted from measured I-V characteristics, Φ_{BI}, was found to differ from that extracted using the measured C-V characteristics, Φ_{BC}. As shown in Fig. 5, Φ_{BI} is smaller than Φ_{BC} and increases with temperature, while Φ_{BC} shows the opposite trend of a slight decrease with increasing temperature. The apparent increase of Φ_{BI} with temperature is attributed to inhomogeneity of the Schottky barrier at the metal-semiconductor interface. For an inhomogeneous barrier (i.e. a metal-semiconductor junction with a spatially-varying Schottky barrier height), the effective barrier height for thermionic emission increases with temperature due to spreading of the energy distribution of the charge carriers [9]. The barrier height extracted from C-V measurements, Φ_{BC}, is governed by depletion region thickness and thus is less sensitive to small-scale inhomogeneity; Φ_{BC} provides an estimate of the average Schottky barrier height in the presence of barrier inhomogeneity [9]. The temperature dependence of Φ_{BF} and Φ_{BC} is qualitatively similar, with Φ_{BC} being slightly smaller than Φ_{BF} due to image force lowering. Image force lowering also gives rise to the more rapid decrease in Φ_{BC} compared to Φ_{BF} with increasing temperature since the sheet carrier concentration as shown in Fig. 4 (and thus the image charge) increases monotonically with temperature.

Based on solution of Poisson's equation, the threshold voltage difference between two temperatures for a pHEMT (ΔV_{th}) can be expressed as [10]

$$\Delta V_{th} = \Delta\Phi_B - \Delta(\Delta E_C) - \Delta\left((q/\varepsilon_s)\int_0^d N_d(x)x\,dx\right) \quad (3)$$

where the symbols are defined as:

- Φ_B Schottky barrier height of the gate;
- ΔE_C conduction band discontinuity between the high bandgap Schottky layer and the low bandgap channel layer;
- ε_s permittivity of the barrier and donor layers;
- N_d effective (ionized) doping concentration of the donor layer;
- d distance between gate and heterointerface.

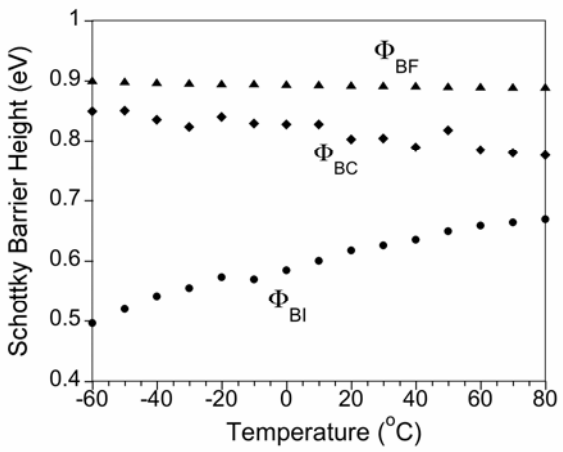

Figure 5. Effective Schottky barrier height extracted from current-voltage measurement (Φ_{BI}), from capacitance-voltage measurement (Φ_{BC}), and the flat-band Schottky barrier height (Φ_{BF}) versus temperature.

Among the available parameters in Eq. 3, the observed threshold voltage shift is expected to be explained by a combination of the change with temperature of the Schottky barrier height, effective doping density, and conduction band discontinuity. Since pinch-off of drain current is governed by the gate depletion region, the Schottky barrier from C-V measurements, Φ_{BC}, is the most natural choice for use in Eq. 3. As shown in Fig. 3, the threshold voltage shifts to more negative values by 42 mV over the temperature range from –60 °C to 80 °C, while Fig. 5 shows that Φ_{BC} decreases by 38 mV over this same range. Thus the change in Φ_{BC} accounts for all but 4 mV of the observed change in threshold voltage from -60 °C to 80 °C. Due to the small ionization energy of Si dopants in InGaP and the sizable ΔE_c between the InGaAs channel and InGaP donor layer, nearly complete ionization and thus only a very small shift in threshold voltage is expected from the doping term in Eq. 3. The conduction band discontinuity is also not expected to change significantly over this limited temperature range. Consequently, the dominant factor in the temperature dependence of the threshold voltage is the dependence of the Schottky barrier height on temperature, which originates not in the semiconductor device structure but rather in the inhomogeneity of the gate metal-semiconductor contact. The presence of a thin interfacial layer from grain boundaries in the metal [11] as well as intermetallic phases formed between Ti and the InGaP Schottky layer [12] may be the root cause of the Schottky barrier inhomogeneity.

CONCLUSION

The temperature dependence of InGaP-based pHEMTs has been examined. The results indicate that the source access resistance is governed by competing increases in carrier concentration and decreases in electron mobility, and similarly the transconductance is controlled

by the temperature dependence of n_s and v_{sat}. The threshold voltage shift with temperature is well explained by the Schottky barrier height's dependence on temperature, and the spatial inhomogeneity of the metal-semiconductor interface likely contributes to the observed barrier behavior and particularly its dependence on temperature.

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ACRONYMS

pHEMT: pseudomorphic high electron mobility transistor
MMIC: monolithic microwave integrated circuit
MOCVD: metal-organic chemical vapor deposition
TLM: transmission-line method
RTA: rapid thermal annealing