Beyond CMOS: Logic Suitability of $In_{0.7}Ga_{0.3}As$ HEMT

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ABSTRACT

We have fabricated 100 nm InAlAs/InGaAs HEMTs that feature a tunneling cap designed to minimize parasitic resistance. We have characterized these devices from the point of logic, studying figures of merit such as gate delay (CV/I), subthreshold slope (S), drain-induced barrier lowering (DIBL), and I_{ON}/I_{OFF}. We have found that these devices exhibit promising logic characteristics. In particular, 100 nm L_g devices yield DIBL as low as 80 mV/V, S of 77 mV/decade, and I_{ON}/I_{OFF} ratio in excess of 10^3 with a gate delay of about 1.2 ps. We have also found that these devices, from a logic application point of view, at 100 nm gate length have reached their scaling limit. Realizing the logic potential of $In_{0.7}Ga_{0.3}As$ HEMTs will require a more scalable device design with better electrostatic integrity. If this can be accomplished, InGaAs HEMTs could well be the technology of choice when the CMOS roadmap comes to end.

INTRODUCTION

Moore's law has been a guiding principle for the semiconductor industry for over 30 years [1]. Sustaining Moore's law requires continuous scaling of Si-transistors. In the current 65 nm technology node, the physical gate length of a Si MOSFET is about 30 nm. This dimension is expected to reach about 10 nm by 2011 [2]. This is broadly believed to be the ultimate limit for CMOS scaling [2]. Identifying a new semiconductor logic device technology is becoming increasingly pressing. Often mentioned candidates are carbon nanotube (CNT) transistors, semiconductor nanowires and, further out, spintronics [3-5]. Unfortunately, many of these device concepts are hardly beyond the prototyping stage.

In contrast, III-V FETs and in particular InAlAs/InGaAs high electron mobility transistors (HEMTs) closely lattice matched to InP constitute a very real device technology that is worth considering. For the last almost 20 years, InAlAs/InGaAs HEMTs have held the world record of frequency response, as measured by cutoff frequency (f_T), with a current record of 562 GHz [6]. This technology is also space qualified [7], and it is being actively considered for future optical fiber systems with transmission speeds in excess of 160 Gb/s [8]. Endowed with extraordinary electron transport properties, it seems imperative to evaluate the potential of InGaAs HEMTs for future beyond-CMOS logic applications.

In spite of all the progress realized in the last decade in this technology, until recently there has not been an analysis of the suitability of InGaAs HEMTs for logic applications. Figures of merit relevant to logic, such as logic gate delay (CV/I), I_{ON}/I_{OFF}, Drain-Induced Barrier Lowering (DIBL) and subthreshold slope (S), have not been evaluated in this family of devices. Recently, we have studied these figures of merit in 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs [9]. In spite of the fact that these devices were not optimized for logic operation, we found that they show substantial promise for logic.

In this work, we have designed and fabricated 100 nm InAlAs/InGaAs HEMTs that feature a tunneling cap designed to minimize parasitic resistance and enhance logic operation. These devices offer excellent logic performance. However, at 100 nm gate length, we find that they have reached their scaling limit. Further gate length scaling will require aggressive insulator thickness scaling.

PROCESS TECHNOLOGY

Figure 1 shows the epitaxial layer structure which was used in this work. This was grown by molecular-beam-epitaxy. It features a strained $In_{0.7}Ga_{0.3}As$ subchannel in order to enhance electron transport. It also includes a 6 nm InP layer which acts as good gate recess etch-stopper as well as good surface passivation layer [10]. In addition, this structure features a multicap layer structure designed to yield extremely low parasitic source and drain resistance (R_S and R_D) which is critical for logic [11][12]. This includes a 5 nm strained and heavily-doped $In_{0.65}Ga_{0.35}As$ cap to reduce metal-to-semiconductor contact resistance and 15 nm heavily-doped $In_{0.52}Al_{0.48}As$ subcap to lower the energy potential barrier with the undoped $In_{0.52}Al_{0.48}As$ insulator layer in the source and drain access region. This will be discussed in more detail below. The Hall mobility ($\mu_{n,Hall}$) and 2-DEG sheet carrier concentration (n_s) for this sample were around 11,000 cm^2/V-sec and $3.0 \times 10^{12}/cm^2$ at room temperature, respectively.

n+ Cap	$In_{0.65}Ga_{0.35}As$	5 nm
	$In_{0.53}Ga_{0.47}As$	15 nm
	$In_{0.52}Al_{0.48}As$	15 nm
Stopper	InP	6 nm
Barrier	$In_{0.52}Al_{0.48}As$	8 nm
δ-doping	Si	-
Spacer	$In_{0.52}Al_{0.48}As$	3 nm
Channel	$In_{0.53}Ga_{0.47}As$	2 nm
	$In_{0.7}Ga_{0.3}As$	8 nm
	$In_{0.53}Ga_{0.47}As$	3 nm
Buffer	$In_{0.52}Al_{0.48}As$	500 nm
3 Inch S. I. InP Substrate		

Fig. 1 $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ epitaxial layer structure.

Device fabrication began with mesa isolation by means of wet chemical etching. This was followed by Ni/Ge/Au evaporation, lift off to form source and drain ohmic contacts with 2 μm spacing, and alloying at 320°C in N_2 ambient.

Electron-beam lithography was applied to make an 100 nm long T-gate, using a conventional double-exposure_and_double-development scheme and a tri-layer resists stack made out of PMMA/PMGI/PMMA. In order to study device scaling, we fabricated devices with gate lengths between 350 nm and 100 nm. Gate recessing was performed following a two-step_recess approach, originally proposed by Suemitsu *et al.* [13]. We removed the cap layer using a mixture of citric acid and H_2O_2. After some over-etching, the InP etch-stopper was an-isotropically removed by Ar-based RIE. Figure 2 shows SEM images of the cross-section of the gate structure before and after Schottky metallization for an 100 nm gate length device.

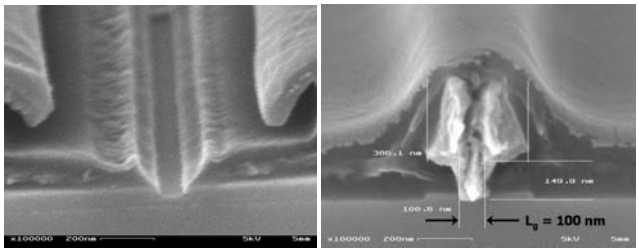

Fig. 2 SEM images: (a) resist profile and (b) T-gate profile.

In order to obtain extremely low R_s, it is crucial to minimize the internal barrier resistance (R_{ins}) as well as the contact resistance (R_c). Figure 3 (a) describes a specially devised TLM structure with the cap etched that we have fabricated to study parasitic resistances in this device. Figure 3 (b) shows both the TLM measurement results on a conventional TLM and on the TLM with the cap etched with a gap of L_{rec} = 1.4 μm. From a conventional TLM structure, we can see that our composite n^+ cap structure yielded an extremely low R_c value of 0.034 Ω –mm, which arises from the use of an InAs-rich n^+-$In_{0.65}Ga_{0.35}As$ cap layer. According to the Hall measurement and 1D simulations for this epi_wafer, the sheet resistance associated with the cap can be estimated to about 80 Ω /sq. This is much less than that of the channel (200 Ω /sq). We can therefore assume that most of the current flows latterally along the cap in the access region and then down to the channel, rather than down from the ohmic to the channel layer and then laterally through the channel. In this model, R_{ins} can be accurately extracted from these two TLM structures. In our case, we get R_{ins} = 0.015 Ω –mm. This extremely low value is attributed to the lowering of the internal potential barrier through the undoped $In_{0.52}Al_{0.48}As$ insulator layer which arises from the use of a heavily doped 15 nm $In_{0.52}Al_{0.48}As$ subcap. Interestingly, we can see that both TLM results show almost the same sheet resistance (R_{sh}) of 77 Ω -mm, which confirms that the initial assumption of carrier flowing through the cap is valid. From this analysis, the devices are expected to have a source resistance (R_s) of about 0.14 Ω –mm (L_{GS} = 1 μm).

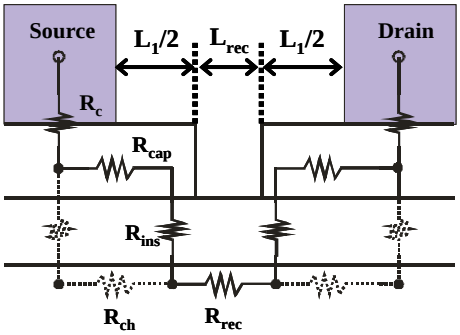

Fig. 3 (a) Schematic of TLM structure with cap etched.

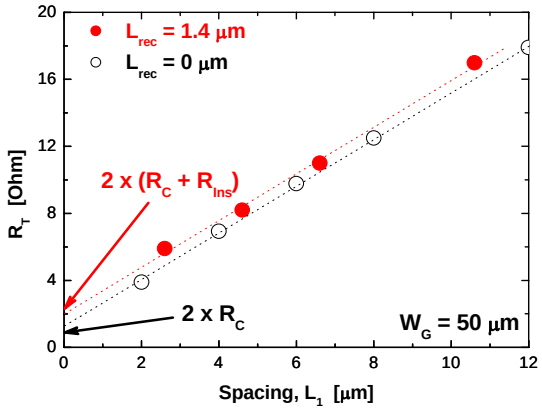

Fig. 3 (b) Resistance measurements in a conventional TLM (empty circles) and a TLM with the cap etched (closed circles).

RESULTS

Figure 4 shows the output characteristics of the fabricated $In_{0.7}Ga_{0.3}As$ HEMTs with the three different gate lengths (100 nm, 250 nm and 350 nm). Reducing gate length appears to result in increased current driving capability. Figure 5 shows the transconductance characteristics of the fabricated $In_{0.7}Ga_{0.3}As$ HEMTs, at a V_{DS} of 0.5 V. The 100 nm device is shown to have a maximum transconductance ($G_{M,max}$) of 1.02 S/mm, which is an excellent value at this drain bias. Interestingly, $G_{M,max}$ improves very little with scaling down below 250 nm. This is due to short-channel effects which are also seen in the negative shift in the threshold voltage (V_T) with gate length.

Figure 6 shows the subthreshold characteristics of the fabricated $In_{0.7}Ga_{0.3}As$ HEMTs with the three different gate lengths, at a V_{DS} of 0.5 V. This figure reveals a very sharp subthreshold slope and a very low off-state current that is mostly limited by gate leakage current through the Schottky gate. The slight softening of the subthreshold slope as L_g approaches 100 nm is another manifestation of short-channel effects.

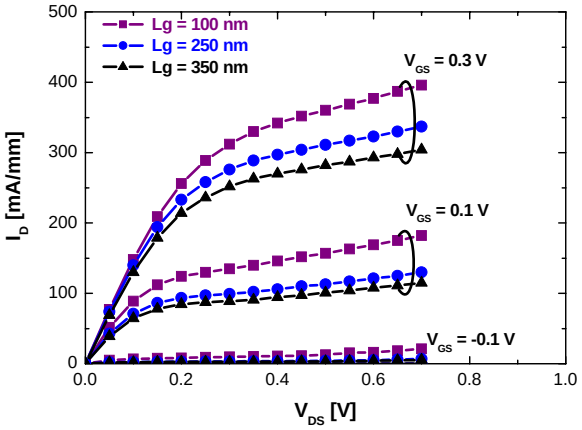

Fig. 4 Output characteristics of $In_{0.7}Ga_{0.3}As$ HEMTs of different gate lengths (L_g = 100, 250 and 350 nm).

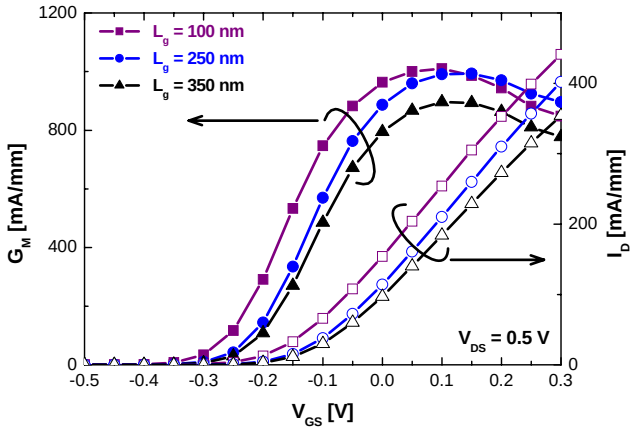

Fig. 5 Transconductance (G_M) and drain current (I_D) characteristics (I_D) of $In_{0.7}Ga_{0.3}As$ HEMTs.

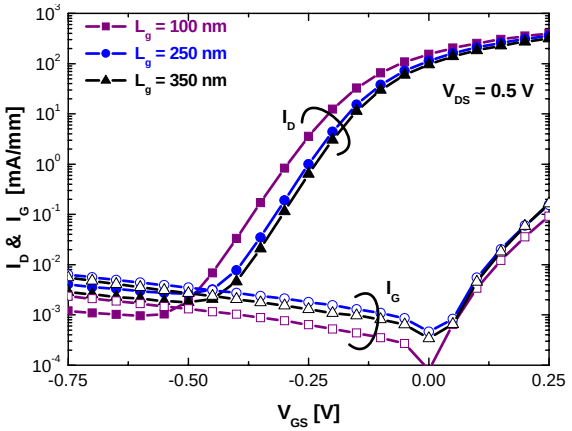

Fig. 6 Subthreshold characteristics of $In_{0.7}Ga_{0.3}As$ HEMTs.

In order to benchmark this semiconductor technology against advanced Si CMOS, careful attention must be paid in the evaluation of logic parameters such as subthreshold slope (S), drain-induced-barrier-lowering (DIBL) and I_{ON}/I_{OFF} ratio. For non-optimized devices, arbitrary selection of V_T and I_{ON} can easily result in an over-estimation of these logic parameters. In our work, we have followed the procedure suggested by Chau [14], which is based on an evaluation methodology for carbon nanotube transistors with non-optimized V_T, suggested by Lundstrom [15]. First, we defined the threshold voltage as the value of V_{GS} for which the drain current is 1 mA/mm at $V_{DS} = V_{CC}$. Then, we selected I_{ON} as 2/3 V_{CC} above V_T, and I_{OFF} as 1/3 V_{CC} below. In our case, V_{CC} is 0.5 V. Table 1 summarizes the results. Indeed, the 100 nm device exhibits a subthreshold slope of 77 mV/decade and DIBL of 80 mV/V (both defined at 1 mA/mm of current) with an I_{ON}/I_{OFF} ratio in excess of 10^4. These are all excellent values that bode well for the logic prospects of this technology. However, we can clearly see that these figures of merit are not scaling properly. For example, in reducing L_g down to 100 nm, V_T shifts severely while DIBL and S degrade, and I_{ON}/I_{OFF} ratio drops by half.

In addition to the static measurement and characterization of our devices, we have also analyzed microwave performance by taking measurements of small-signal S-parameters from 1 to 40 GHz. Our devices showed maximum f_T and f_{max}, of 231 GHz and 190 GHz, respectively, at a V_{DS} of 0.5 V. These are excellent values at this low bias voltage.

L_g [nm]	DIBL [mV/V]	S [mV/dec.]	I_{ON}/I_{OFF}
350	53	73	4.0×10^4
250	58	73	3.3×10^4
100	80	77	1.5×10^4

Table. 1 Extracted logic parameters at a V_{DS} of 0.5 V.

DISCUSSION

In order to understand the significance of the results obtained in this work, we have compared the logic figures of merit that we have extracted against those of state-of-the-art Si MOSFETs. Figure 7 compares the subthreshold slope of our $In_{0.7}Ga_{0.3}As$ HEMTs to that of advanced Si MOSFETs as a function of gate length. In our devices, the subthreshold slope is extracted at a V_{CC} of 0.5 V. Both technologies exhibit almost equivalent subthreshold slopes.

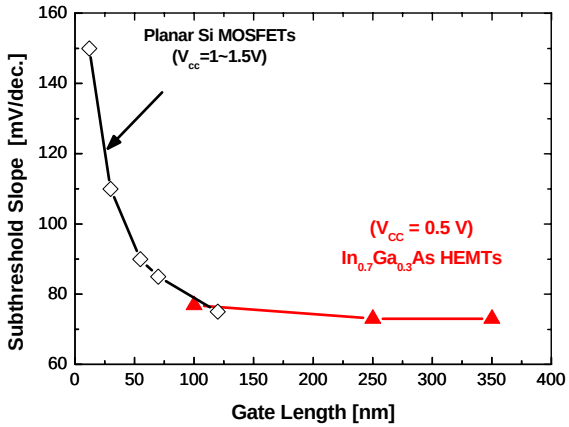

Fig. 7 Subthreshold slope vs. gate length for our $In_{0.7}Ga_{0.3}As$ HEMTs at a V_{CC} of 0.5 V and state-of-the-art planar-type Si-MOSFETs at V_{CC} of 1-1.5 V [14].

A comparison of relative logic circuit speed between InGaAs HEMTs and Si MOSFETs can be obtained by estimating the gate delay, or CV/I. In this, C is the total gate capacitance which was extracted from small-signal S-parameter measurements. V and I are the supply voltage, V_{CC}, and the on-current, I_{ON}, respectively [14]. Figure 8 plots CV/I for our 100 nm HEMT, a state-of-the-art Si-MOSFET [14] and a recent InSb HEMT [16], as a function of I_{ON}/I_{OFF}. For a given device, the various points result from different definitions of V_T. This kind of plot, therefore, allows the comparison of devices that have a non-optimized threshold voltage. This figure clearly shows that our $In_{0.7}Ga_{0.3}As$ HEMTs deliver excellent logic gate delay and a very high I_{ON}/I_{OFF} ratio, at the same time.

Figure 9 shows the gate delay as a function of gate length (L_g) for all the devices in Fig. 8. For our device, we have selected the gate delay associated with the V_T definition that yields an I_{ON}/I_{OFF} ratio of 10^3. Our 100 nm $In_{0.7}Ga_{0.3}As$ HEMTs exhibit a gate delay of 1.16 ps which is about a factor of 2 times better than equivalent Si-MOSFETs. This excellent result arises from the superior electron transport properties of our heterostructure.

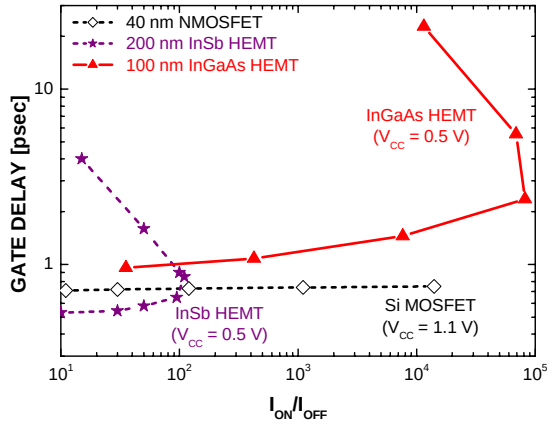

Fig. 8 Logic gate delay vs. I_{ON}/I_{OFF} for our InGaAs HEMTs, state-of-the-art Si-MOSFETs [14] and InSb HEMTs [16].

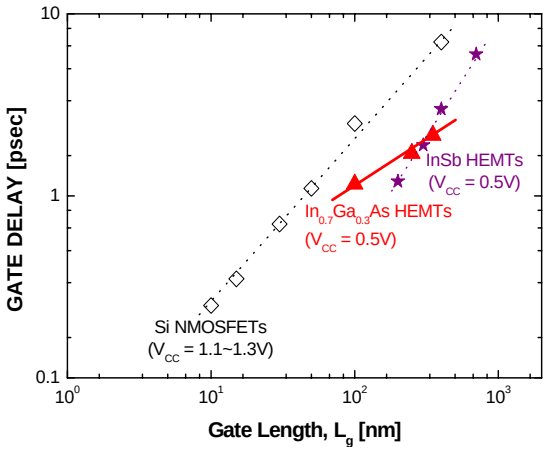

Fig. 9 Logic gate delay vs. gate length for our InGaAs HEMTs, state-of-the-art Si-MOSFETs [14] and InSb HEMTs [16]. In our devices, CV/I was chosen to have I_{ON}/I_{OFF} ratio of 10^3.

While the logic characteristics of our 100 nm $In_{0.7}Ga_{0.3}As$ HEMTs are impressive, prospects for improvements through further gate length scaling do not appear promising. As Table I shows, scaling down to 100 nm, $G_{M,max}$ no longer improves and V_T begins to shift significantly in the negative direction. More importantly, DIBL and I_{ON}/I_{OFF} ratio significantly degrade. All this means that at 100 nm, this device design has reached its ultimate scaling limit. Further gate length scaling will require improving the electrostatic integrity of the device through aggressive insulator thickness scaling. The key trade-off in accomplishing this is potentially high gate leakage current that will add to the off-state current. Mitigating this will require innovative device engineering.

CONCLUSIONS

In summary, we have studied the logic suitability of $In_{0.7}Ga_{0.3}As$ HEMTs focusing on figures of merit that are relevant for logic operation, such as gate delay (CV/I), subthreshold slope, DIBL and I_{ON}/I_{OFF}. We have found that our $In_{0.7}Ga_{0.3}As$ HEMTs exhibit very promising logic characteristics. In particular, 100 nm L_g devices exhibit I_{ON}/I_{OFF} ratios in excess of 10^3 with a gate delay of about 1.2 ps, at a V_{CC} of 0.5 V. Realizing the logic potential of $In_{0.7}Ga_{0.3}As$ HEMTs will require a new device design with better electrostatic integrity. With further device optimization in the form of scaled insulator thickness, positive V_T and a self-aligned gate design, InGaAs HEMTs could well be the technology of choice when the CMOS roadmap comes to an end.

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REFERENCES

[1] G. E. Moore, *Electronics*, 1965.
[2] M. T. Bohr, *IEEE Trans. Nanotechnology*, pp. 56-62, 2002.
[3] S. J. Wind, *et al.*, *Appl. Phys. Lett.*, pp. 3817-3819, 2002.
[4] M. Radosavlevic, *et al.*, *Appl. Phys. Lett.*, pp. 2435-2437, 2003.
[5] L. J. Lauhon, *et al.*, *Nature*, Vol. 420, pp. 57-61, 2002.
[6] Y. Yamashita, *et al.*, *IEEE EDL*, pp. 573-575, 2002.
[7] D. Streit, *et al.*, in *IEEE IPRM Conference*, pp. 11-14, 2002.
[8] K. Murata, *et al.*, *IEEE JSSCC*, pp. 207-213, 2004.
[9] D.-H. Kim, *et al.*, *IEDM*, pp. 455-458, 2005.
[10] D.-H. Kim, *et al.*, *IEDM*, pp. 1027-1030, 2004.
[11] R. Chau, *et al.*, *Physica E*, pp. 1-5, 2003.
[12] K. J. Chen, *et al.*, *IEEE TED*, pp. 252-257, 1996.
[13] T. Suemitsu, *et al.*, *IEEE TED*, pp. 1074-1080, 1999.
[14] R. Chau, *et al.*, *IEEE Trans. Nano.*, pp. 153-158, 2005.
[15] J. Guo, *et al.*, *IEDM*, pp. 703-706, 2004
[16] T. Ashley, *et al.*, *CS-MANTECH*, 2005.

ACRONYMS

HEMT: High Electron Mobility Transistor
DIBL: Drain Induced Barrier Lowering
TSR: Two Step Recess