InP/InGaAs DHBT Large Signal Model for Nonlinearity Harmonic Predictions in ICs

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Abstract

In this work an improved large-signal transistor model is developed especially for InP DHBTs based on Agilent ADS SDD model platform. This model includes the nonlinear effects of current blocking and velocity modulation. The model is verified on Vitesse VIP2 300GHz InP/InGaAs DHBTs and the simulation results of different models are compared with measured results. In addition to the validation of single devices, integrated circuits were designed and measured. It is shown that the model presented in this paper has more accurate predictions in circuit nonlinearity than conventional VBIC results.

INTRODUCTION

An accurate model for transistors at radio frequency range is critical to the modern design of high-performance and high-frequency integrated circuits. InP based heterojunction bipolar transistor (HBT) technology has been recognized to have high potential for the applications of ultra high speed analog-mixed signal circuits [1],[2]. Currently the most popular transistor model used for commercial purposes is the VBIC model, which is developed on Si devices. However, a Si-based transistor model is not sufficient to model the Type-I InP DHBTs due to the additional mechanisms in III-V devices. Therefore, in this work an improved large-signal transistor model is developed especially for Type-I InP DHBTs based on Agilent ADS SDD model platform.

The model presented in this paper focuses on the nonlinearity effect of Type-I DHBT, including current blocking and velocity modulation. Because InP substrate has a poorer thermal conductivity than Si, the thermal effects of InP HBT become critical. Therefore, the thermal model in this work covers device self-heating effect to account for the actual performance of the device.

The model is first verified in a single device. Good DC fittings are achieved up to the region of high current injection. The model also fits high-frequency measured data well at various bias conditions. The fall-off trends of device unity current gain cutoff frequency f_T and maximum oscillation frequency f_{MAX} are better predicted by the improved model than by VBIC model.

In addition to the characterization of a single device, an integrated circuit, variable gain amplifier (VGA), is also designed and fabricated to verify the model accuracy. The linearity predictions of it are significantly improved by our proposed model at frequencies up to 40GHz in comparison with VBIC model.

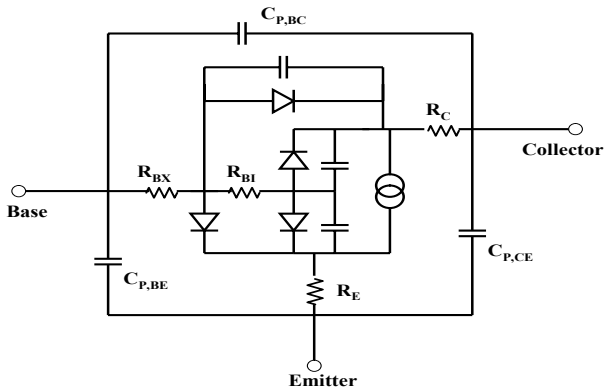

Figure 1. Topology of the DHBT large-signal model

INP DHBT LARGE SIGNAL MODEL

In this work, the model is developed using Vitesse VIP2 InP/InGaAs DHBT technology. Several special process features were developed to make compact and highly scalable devices and to improve the manufacturability [3]. A transistor with emitter size of 0.5x4.0μm^2 has 300GHz f_T and 337GHz f_{MAX}. The peak f_T occurs at current density of 500kA/cm^2.

The improved InP DHBT model has been developed using SDD (Symbolically Defined Device) model in ADS environment. Figure 1 shows the complete topology of the proposed large-signal model for Type-I DHBT. It is based

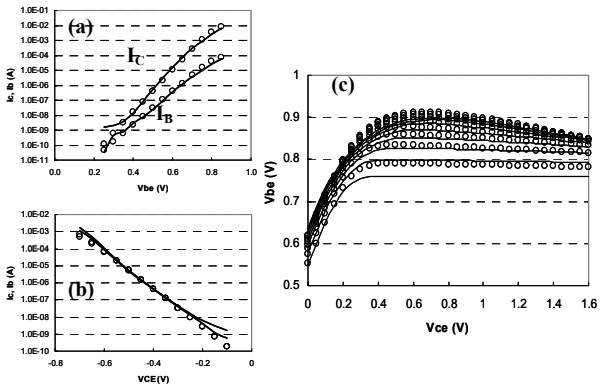

Figure 2. Modeling results of large-signal model developed in this work for 0.5 x 4.0μm^2 VIP2 InP/InGaAs DHBT. The solid lines represent measured data and the circle marks represent the model data. (a) Gummel plot, (b) reverse Gummel plot, and (c) V_{BE} curves vs. V_{CE}.

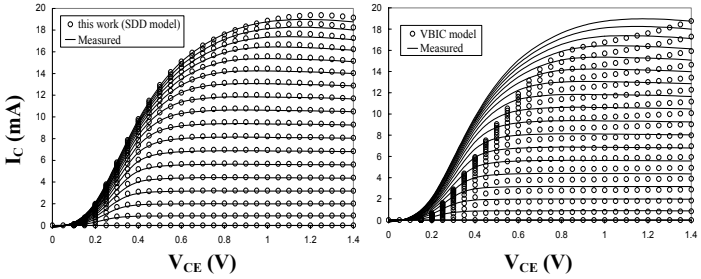

Figure 3. The measurement data of 0.5 × 4.0 μm^2 VIP2 InP/InGaAs DHBT compared with the simulations of model developed in this work (left) and the VBIC model (right).

on Gummel-Poon integral charge control model and incorporates many physical mechanisms, including self-heating, dc current blocking, velocity modulation, Early effect, Kirk effect and peripheral parasitics.

One of the most important physical effects of III-V DHBTs is current blocking. The rising of energy band at high current density can block electron transport by band energy discontinuity or affect electron drift velocity in collector transport. The I_C-V_{CE} curves of the DHBT device show a knee round-off especially at high current density, which indicates DC current blocking effect. This effect is equivalent to an increase in collector resistance and thus is modeled by a bias-dependent collector resistor in this work. Also, depending on material designs, the effects of current blocking and velocity modulation can have different weightings to affect the device high-frequency performance. Therefore, these effects should be considered into device modeling in a general way. A simplified equation for collector transit time is thus introduced into the proposed model given by [4]

$$\tau(i_C) \approx \frac{1+i_C^m}{1+i_C^n} \qquad (1)$$

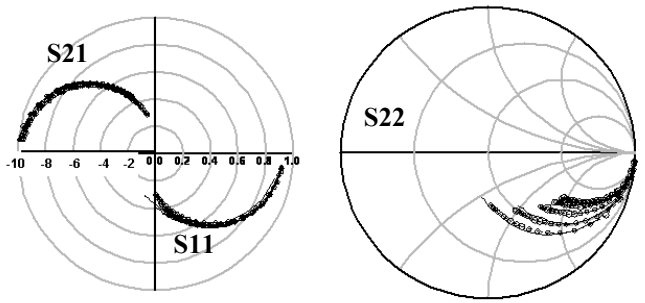

Figure 4. Measured and modeled S-parameters of 0.5 x 4.0μm^2 InP DHBT at V_{CE} = 0.6-1.6V, J_C = 2.1mA/μm^2. The solid lines represent measured data and the circle marks represent the model data.

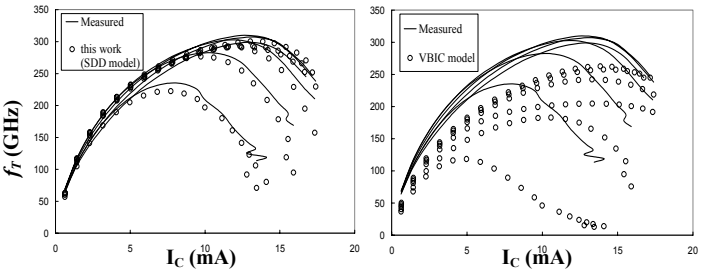

Figure 5. Measured and modeled f_T as a function of collector current for 0.5 × 4.0 μm^2 VIP2 InP/InGaAs DHBT. The model developed in this work (left) shows better f_T trend fittings than VBIC model (right) does.

In Eq. (1), m and n are modeling parameters to reflect the variation trend of collector transit time $\tau(i_C)$ in the function of current density i_C. If m > n, the transition delay increases with current due to current blocking and if m < n, the transit time drops due to velocity modulation. By integrating the equation with respect to the collector current, a more accurate relation for the base-collector junction charge is obtained [4].

The temperature rise over the ambient temperature resulting from device self-heating is defined by a thermal RC circuit. The corresponding thermal parameters are extracted from the measured data of various substrate temperatures (25°C, 50°C, and 75°C). Therefore, the shift of bias condition due to temperature rise in circuit operation can be properly modeled.

Figure 2 shows the DC modeling results of a 0.5x4.0μm^2 Vitesse VIP2 InP/InGaAs DHBT. The Gummel plot, as well as reverse Gummel plot is well fitted. This indicates proper parameter extractions for both base-emitter and base-collector junctions. The characteristic that V_{BE} declines with respect to V_{CE} due to self-heating is also well modeled.

The comparison of device I-V curves between VBIC model and the proposed model is shown in Figure 3. The VBIC model has been wildly used in SiGe technology and implemented in most of important design environments. The parameters of VBIC model are provided in Vitesse design kit V1.1.4 for Cadence environment. VBIC model utilizes Kull's model as the framework of base-collector charge [5],

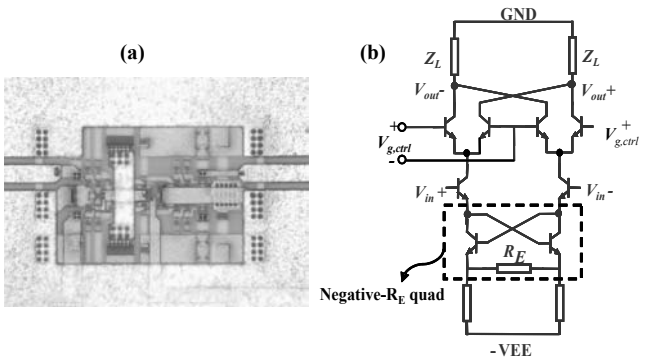

Figure 6. (a) Photograph of the core high-gain, wideband VGA (b) schematic of the modified Gilbert cell using negative resistance

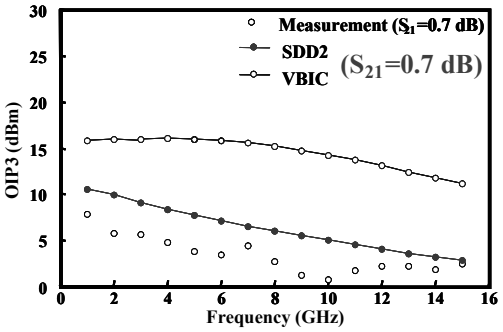

Figure 7. One-tone measured and modeled results when the gain is 0.7dB.

[6]. Kull's model is focused on the description of silicon in which electron velocity gradually saturated along with increasing electric field without overshooting. It is shown that VBIC model cannot fit the knee voltages and I_C-V_{CE} curves well while good agreement between measurement and model data is achieved by the new proposed model.

The ac performance of the InP HBT is characterized from 500MHz to 50GHz using HP8510C network analyzer. Figure 4 shows the measured and modeled S-parameters of the 0.5x4.0μm^2 DHBT. It is biased at current density J_C = 2.1mA/μm^2 with V_{CE} = 0.6 to 1.6V. By the analytical expressions of the interception point of second and third harmonic derived in [7], it is shown that there is a direct relation between nonlinearity and transistor f_T. Therefore, very good fit of the cutoff frequency versus bias voltage and collector current is required in order to achieve accurate distortion simulations.

Good predictions of the sharp f_T falloff with increasing collector current are achieved by the proposed model due to the empirical equation of electron transit time as a function of collector current, which accounts for the current blocking and velocity modulation effects. The transistor f_T is shown in Figure 5 in comparison with SDD and VBIC models. It is observed that the sharp cut-off frequency drop at high current density region cannot be described by VBIC model.

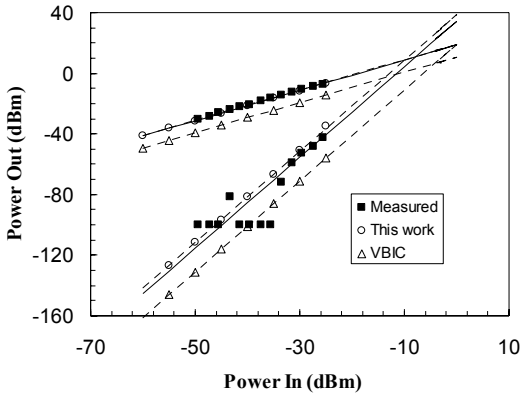

Figure 8. Two-tone measurement data at 30GHz with 19dB VGA gain. VBIC and SDD model simulation results are compared.

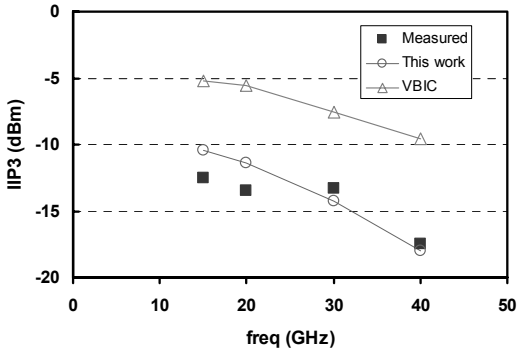

Figure 9. Model comparison of the two-tone nonlinearity results when the VGA gain is 21dB.

MODEL VALIDATION IN CIRCUIT LEVEL

In order to verify the model accuracy at circuit level, a variable gain amplifier (VGA) was designed and fabricated using Vitesse VIP2 technology. The conventional VGA is based on Gilbert multiplier. By changing the base voltage of the upper transistors, the collector current and thus the transconductance g_m is changed, which leads to the controllable small signal gain. In this design, two cross coupled transistors are inserted as part of the emitter degeneration (Figure 6) [8]. It generates equivalent negative resistance and increases the gain without the penalty of decreasing bandwidth. Therefore, a record-high gain-bandwidth product of > 520GHz has been achieved [4]. Meanwhile, special cares have to be taken to ensure stability of this design [8].

Figure 6 shows the picture of the fabricated VGA chip. It has totally 66 transistors and four levels of aluminum interconnection. First, one-tone measurement is taken at lower frequencies up to 15GHz. Figure 7 is the one-tone measurement results compared with model simulations from 1 to 15GHz when VGA gain is 0.7dB. The proposed SDD model better predicts the OIP3 than VBIC does by 5 ~ 10dB.

Two-tone measurements are also performed to characterize the circuit nonlinearity by using Agilent 8565E spectrum analyzer for signals up to 50GHz. Figure 8 shows

the power measurement results compared with simulations using VBIC and our proposed model. It is measured at 30GHz with 19dB gain. It is shown that VBIC model tends to underestimate the power of the third harmonic by more than 10dB while our new proposed model can fit closely to the measured third harmonic.

Another comparison is made from 15GHz to 40GHz input frequency (Figure 9). The bias condition is fixed at $V_{g,ctrl} = 0.21V$, which corresponds to 21dB small-signal gain. The nonlinearity predicted by the new SDD model is much more accurate than by VBIC model over the entire measured frequency range. The improvement can be as large as 8dB at high frequency.

In this VGA design, the model accuracy around knee voltage becomes critical to linearity prediction because this circuit uses negative resistance quad that is biased at knee voltage. The cross-coupled transistors are placed at the emitter node and thus are closely related to the circuit linearity. SDD model has the advantage of better fittings of knee round-off than VBIC because of the DC and RF modeling of current blocking effect. Therefore, SDD shows more accurate harmonic predictions.

CONCLUSIONS

In this paper, a new modeling approach is proposed for InP/InGaAs Type-I DHBT. The nonlinear effects in base-collector junction, including current blocking, velocity modulation and device self-heating are incorporated into the model. The proposed model is verified at both device and circuit levels. The DC and RF fittings of a single 0.5μmx4.0μm Vitesse InP DHBT are achieved over various bias conditions. A variable gain amplifier was designed and fabricated and its linearity performance was measured. The proposed SDD model significantly improves the predictions of third-order harmonic distortion for frequencies up to 40GHz.

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REFERENCES

[1] H. Fukuyama, K. Sano, M. Ida, K. Kurishima, K. Murata, K. Ishii, T. Enoki, and H. Sugahara, "InP/InGaAs DHBT parallel feedback amplifier with 14-dB gain and 91-GHz bandwidth," in *Proc. Int. Conf. Indium Phosphide Related Materials*, Kagoshima, Japan, May 2004, pp.659-662.

[2] D. Caruth, S.C. Shen, D. Chan, M. Feng, and J. Schutt-Aine, "A 40 Gb/s integrated differential PIN+TIA with DC offset control using InP SHBT technology," 2002 GaAs IC 24th Annual Technical Digest, pp. 59-62,2002.

[3] M. Le, G. He, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee, J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J. W. Lai, and M. Feng, "Self-aligned InP DHBTs for 150GHz digital and mixed signal circuits," in *Proc. Int. Conf. Indium Phosphide Related Materials*, Glasgow, Scotland, UK, May 2005.

[4] J.W. Lai, D. Caruth, Y.J. Chuang, K. Cimino, R. Elder, D. Jansen, F. Stroili, M. Le, and M. Feng, "300 GHz InP DHBT large signal model including current blocking effect and validated by Gilbert multiplier circuits," 2005 CSIC 27th Annual Technical Digest, pp.61-64, 2005.

[5] C. McAndrew, J. Seitchik, D. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, P. van Wijnen, and L. Wagner, "VBIC95: an improved vertical, IC bipolar transistor model," in *Proc. IEEE BCTM*, pp.170-177, 1995.

[6] G. Kull, L. Nagel, S.-W. Lee, P. Lloyd, J. Prendergast, and H. Dirks, "A unified circuit model for bipolar transistors including quasi-saturation effects," *IEEE Trans.Electron Devices*, vol. ED-32, no. 6, June 1985.

[7] H. Poon, "Implication of transistor frequency dependence on intermodulation distortion," *IEEE Trans. Electron Device*, vol. 21, no. 1, pp.110-112, January 1974.

[8] J.W. Lai, Y.J. Chuang, K. Cimino, and M. Feng, "Design of variable gain amplifier with gain-bandwidth product up to 354 GHz implemented in InP/InGaAs DHBT technology," *IEEE Trans. Microw. Theory Tech*., 2005, in press.