Determining Inductor Interactions with a Design of Experiment

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Abstract

A method of designing higher quality (Q) factor inductors is demonstrated in this paper. The method is based on optimizing the fab process for a certain device design. The method can be applied to any IC process. The optimization method shows where the process limits are with respect to a certain device. The analysis shows where process improvements can be made to achieve the desired inductor.

Introduction

Passive devices in transmit modules for mobile wireless devices have many uses including impedance matching and filters. As these modules decrease in size, the need for passive integration becomes more important. Also, passive integration on the GaAs substrate allows for more control of the critical dimensions through thin film deposition and fine lithography. Passive devices include capacitors, resistors, and inductors. The focus here will be on inductors. A method to identify the aspects of GaAs IC backend processes which influence quality factor (Q) (1.9 GHZ) will be shown. The definition for Q is given by

$$Q = (2\pi fL)/R$$

where L and R is inductance and resistance respectively [1]. It is desirable to have as high a Q as possible. An inductor with a higher Q would have less loss than one with a lower Q. When taken into account that efficiency and loss is a main concern when designing components for mobile battery powered devices, the high Q inductor is usually more desirable than the lower Q inductor. This method is ideal for using a current process technology to design an inductor or to design a new backend process in order to be able to fabricate higher Q inductors using a current device design.

Experiment

A mask set was designed with inductors of various designs. In the experiment, two more variations were added. These included inductor metal thickness (MET3) and dielectric thickness. The wafers processed for the DOE consisted of 6 lots of wafers with different combinations of inductor metal thickness and dielectric thickness. Table 1 shows these combinations.

Table 1: Process variations for DOE

Lot	MET3 (μm)	Dielectric (μm)
A	3.4	0.5
B	5.2	2.0
C	6.2	0.5
D	6.5	2.0
E	7.15	0.5
F	7.2	2.0

The MET1 and MET2 thicknesses were identical for all 6 wafer lots. MET1 and MET2 were used for the inductor feeds.

After the wafer processing was completed, the wafers were tested. The inductors from each lot were characterized using an Agilent VEE program. The program controls an Agilent E5270A DC source, an Agilent E8362B PNA Series Network Analyzer, and an Electroglas EG2001 auto-probe. The probes used were Cascade Microtech I-40-A-GSG-100 infinity RF probe tips. The Picoprobe CS-5 calibration substrate was used to do a SOLT calibration up to the reference plane. The short, open, and thru micro strip structures provided the feed structure calibration data. The calibration allows for de-embedding the inductor data. After calibration, the inductors were measured using the same test equipment as was used in the calibration. The Q of each inductor was derived from the de-embedded inductor data.

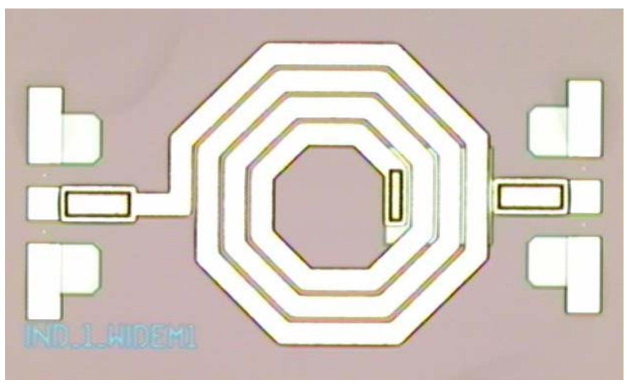

Figure 1: Image of IND_1

Analysis

A complete set of data for each of the inductors was generated from 0.4 GHz to 12.4 GHz in steps of 0.5 GHz. An inductor (IND_1) was chosen for analysis. The other inductors that were tested produced similar results. Three IND_1inductors were tested for each of the 6 lots. The frequency of 1.9 GHz was the point at which the analysis was completed. The statistical software JMP made by SAS was used for the inductor analysis. The modeling function of the software allows the user to study the interactions of the various inductor characteristics.

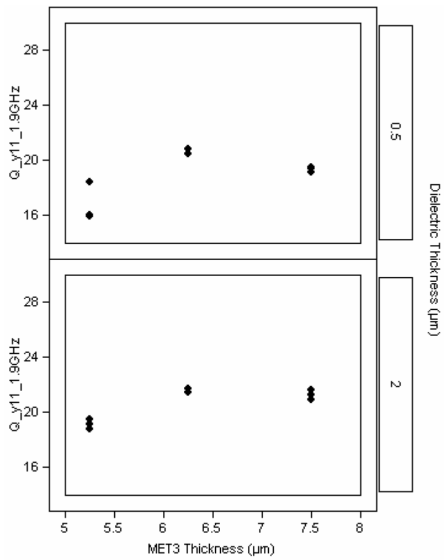

Figure 2: JMP analysis of IND_1 from the 6 lots

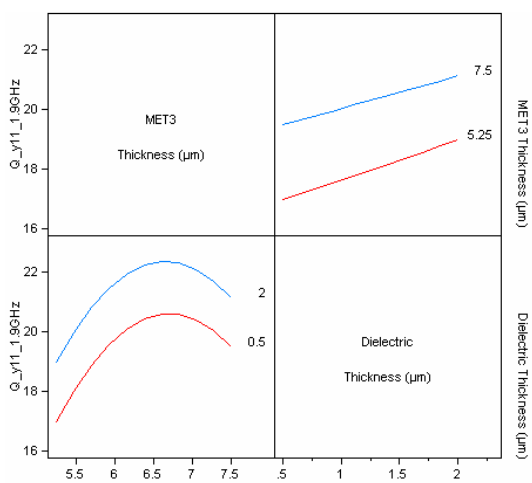

Figure 3: JMP interactions plot of IND_1

The Q analysis of IND_1 shows a higher Q for the 6.25 µm versus 7.5 µm thick inductors in Figures 2 and 3. These results suggest skin depth effects are present. In a planar conductor, high-frequency current exponentially decreases at it penetrates into the conductor. Because current is confined to the surface of the conductor (inductor), loss will increase as the inductor thickness becomes greater than the inductor's skin depth [2]. There are methods to improve Q using similar total thicknesses such as using multi-layered devices which would limit eddy currents [3], but the focus here is on the process and not the design

The inductors with the 2.0 µm dielectric had a higher Q than the 0.5 µm devices. Fewer losses occur beneath the device leading to a higher Q. To increase the Q of this inductor, a dielectric thickness change would be the best solution since a metal change would produce limited results. A dielectric thickness increase would decrease the inductor self-capacitance leading to a higher resonance. This would result in a higher Q. If there are thickness constraints, then a dielectric with a lower permittivity would have to be sought. It would allow for a higher Q without changing the layer dimension.

To diminish any uncertainty over the measured results, a simulation was done using Agilent Technologies' ADS software using the dimensions of IND_1. The results of the simulation are shown in Figure 4 below.

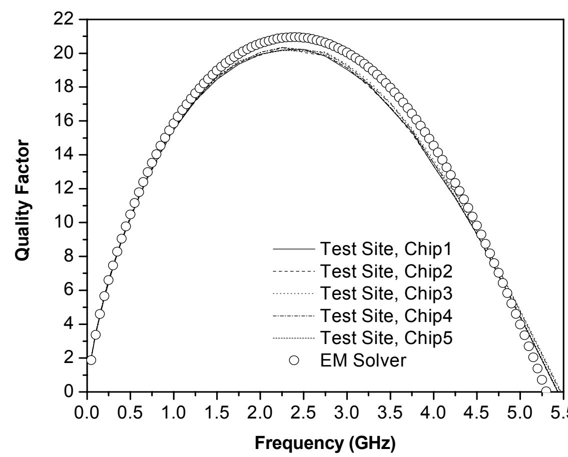

Figure 4: The measured Q versus the simulated Q

Figure 4 shows that the ADS EM solver results coincided well with the calculated results from the measurements.

Conclusion

The method of analysis used in this experiment demonstrates which variation change changes Q the most for an inductor in this process. The experiment also shows that skin depth effects also affect inductors in GaAs IC processes. The method shown can direct the development of a backend process that can focus on the characteristic which can provide the desired inductor electrical characteristics.

References

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Acronyms

IND_1: Name of the inductor analyzed in this paper
MET1: First metal layer
MET2: Second metal layer
MET3: Third metal layer
Q: Quality factor