The First 0.1µm 6" GaAs PHEMT MMIC Process

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Abstract

BAE Systems has developed the world's first 0.1µm 6" 2-mil PHEMT MMIC process with high power, high yield and excellent reliability. Utilizing T-gate technology and 2-mil substrates, we have created a millimeter wave technology producing excellent performance from Ka-band through W-bands. DC and RF characteristics have excellent uniformity across the wafer with very high spec yield. Due to the excellent reliability and performance characteristics, the developed HPA technology provides a low cost advantage for millimeter-wave applications.

INTRODUCTION

There is an increasing demand for high performance millimeter wave (MMW) GaAs technology for both commercial and military electronic applications such as VSAT and phased array radar applications [1]. Currently, VSAT technology operates in the Ku-band but will soon be moving into frequencies within the Ka-band creating a demand for high performing, low cost Ka-band MMICs. Additionally, there is an increasing need for high gain, broad bandwidth SSPAs for W-band operation, a requirement not easily met with current 0.15µm technology [2]. The reported 0.1µm PHEMT technology allows for creation of such SSPA's for military and commercial applications. In order to be competitive, technology-manufacturing paths are driven by cost reduction while maintaining performance. One method is by enlarging the wafer size to provide substantially more area at a lower chip cost (see Table I). Using state of the art equipment designed for the enlarged wafer sizes additionally creates better uniformity, higher yields and lower cycle times. Success of 2µm InGaP HBT and 0.15µm GaAs PHEMT technology has been reported on 6" 4-mil thick wafers [3-7] yet there has been no publication at the time of this paper's generation indicating 6" 0.1µm PHEMT technology.

TABLE I
ANTICIPATED COST ADVANTAGE OF 6" VS. 3" AND 4" PROCESSES (NORMALIZED TO 4")

	3"	4"	6"
Usable Wafer Area*	0.6	1	2.4
Process Cost	1.0	1	1.2
Epi Cost	0.8	1	1.8
Chip Out Per Lot	0.6	1	2.4
Chip Unit cost**	1.6	1	0.6

*Excluding 5mm around edge circumference of wafers due to epi/processing ring.
**Assuming processing cost = 2/3 total cost and epi cost = 1/3 total cost

BAE Systems has developed the first 0.1µm GaAs PHEMT MMIC process on 150-mm (6") substrates (displayed in Figure 1). Although success has been attained on Ka- through W-band MMICs, the focus in this paper will be on one circuit that will be used as a process demonstration vehicle: a balanced V-band MMIC to demonstrate statistical power performance and reliability in comparison with its mature 3" counterpart.

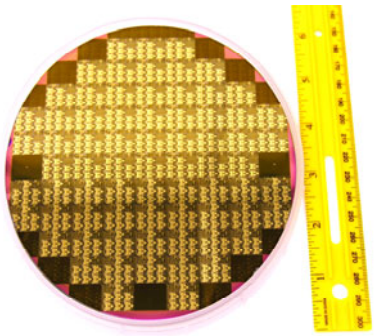

Fig.1: Fully processed 2-mil 6" 0.1µm PHEMT MMIC wafer.

POWER PHEMT TECHNOLOGY

The 0.1µm 6" single-recess (SR) PHEMT MMIC fabrication utilizes mostly cassette-to-cassette equipment in the foundry. The highly automatic wafer processing reduces human wafer handling and improves visual yield. The epitaxial layers are grown via MBE and isolated through mesa etching. Ohmic contacts forming source and drain are formed using a Au-Ge based process with a typical contact resistance of 0.11Ω-mm. TaN is used for 25Ω/square thin film resistors and two metal layers are used for interconnects. 0.1µm T-gates are realized through bilayer resist, e-beam lithography and fully selective etching of the n+ cap, followed by Ti/Pt/Au metallization to form the Schottky junction. An example of a 0.1µm gate on a 6" wafer is given in Figure 2. FETs are passivated using PECVD SiN followed by creation of 400pF/mm^2 MIM. All wafers were fully backside processed using our 2-mil substrate process with small size slot vias to provide direct source grounding for reduced source inductance and improved thermal resistance. The 2-mil via technology is critical for high frequency power operation. Connection to the frontside is achieved with the use of plated Au.

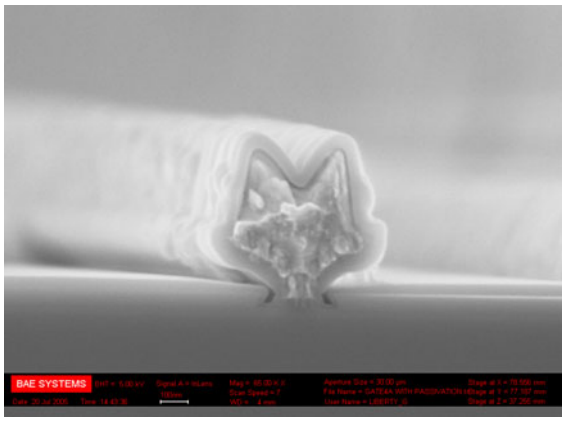

Fig. 2: SEM picture of 0.1µm T-gate showing excellent coverage of SiN passivation.

6" WAFER PROCESSING CHALLENGES

Areas of particular challenge were 0.1µm gate definition, demount of the wafer from its carrier post backside processing and wafer breakage. Gate lithography required precision in process and definition to achieve clean, consistent resist openings (±3%) for uniform 0.1µm gate lengths, good pinchoff and high gate yield. The critical T-gates were defined by a Leica EBPG 5000 e-beam lithography system with a spot size of ~15nm. A new procedure has been developed for demounting to handle the fragile 2mil thin 6" wafers for RF testing. Due to the size of the wafers, breakage is carefully avoided through equipment setup adjustment (optimization) during both front side and backside processing. To clean the thin 2-mil wafers, a process was developed using a special fixture. The combination of automated handling during front side processing with these new procedures led to visual yields ~90%. To validate the 6" 0.1µm process and its reproducibility, 3 lots were processed. Line yield on the three lots was 100%, 90% and 100%, respectively. Breakage of one wafer in the second lot was during front side processing. Investigation of this wafer's pieces led to the conclusion that the cause of breakage was internal stress of the GaAs, possibly from a previous bake.

DEVICE CHARACTERISTICS

BAE Systems 0.1µm single-recess PHEMT is based on a double-heterojunction epi structure with doping on both sides of the InGaAs channel to provide a higher sheet charge density for higher full channel current and output power. Automated electrical testing of key process parameters are tracked using our process control monitor (PCM). Critical parameters such as the full channel current, I_{dss}, G_m, BV_{gd}, V_{po}, device isolation, thin film resistance, and capacitance are measured at different stages of the process. The SR PHEMT exhibits extrinsic transconductance of 570 mS/mm at V_d of 2.5V with $I_{ds,max}$ of 615mA/mm. Off-state gate-drain breakdown was measured to be -11.5V with on-state channel breakdown of 7V (V_{gs} = -0.3V). These DC characteristics are within 95% of the performance levels achieved with our mature 3" process. After completion of MMIC fabrication, wafers are 100% RF tested for Small Signal parameters and power. Table II shows the tight distribution of device DC characteristics as well as the extremely high DC and RF spec yield. Pulsed output I-V characteristics are shown in Figure 3.

TABLE II
UNIFORMITY AND YIELD OF PHEMT DC/RF PERFORMANCE

Parameter	Unit	Value	Spec Yield
Ifull	mA/mm	615 (±3%)	100%
Gm	mS/mm	570 (±6%)	86%
BVgd	V	-11.5 (±5%)	99%
S11	dB	-20 (±2dB)	100%
S21	dB	13.75 (±0.25dB)	94%
Pout in V-band	dBm	27.5 (±0.25dBm)	88%

I_{full}: full channel current at V_{gs}=+0.6V, BV_{gd}: gate-to-drain breakdown voltage at V_{gd}=1ma/mm, g_m: peak transconductance, S11: small signal input return loss, S21: small signal gain

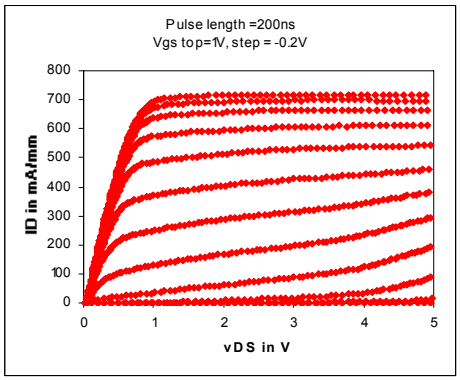

Fig.3: Pulsed I-V of 6" 0.1µm PHEMT

The V-band power MMIC RF characteristics processed on 6" substrates closely resemble those of the same MMICs processed on 3" substrates. The measured small-signal gain is typically 14dB from 59 to 64GHz. The minimum input and output return losses are 20dB. As shown in Figures 4 and 5, the V-band MMICs exhibit output power of 28dBm with PAE of 21%.

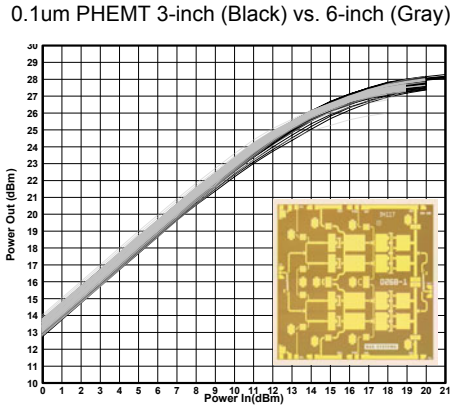

Fig.4: Measured Pout for 6" 0.1µm Power PHEMT MMIC (gray) compared with its typical 3" counterpart (black).
Inset: Balanced V-Band MMIC using 0.1µm 6" power PHEMT technology. (Output stage = 8x200µm)

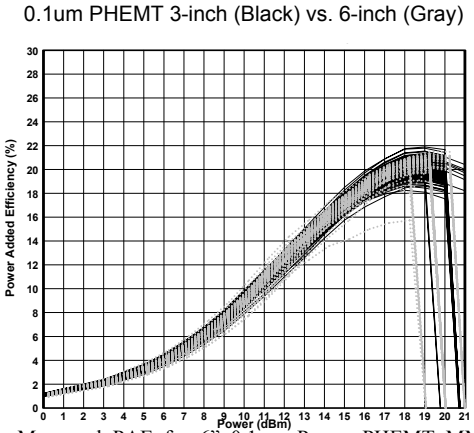

Fig.5: Measured PAE for 6" 0.1µm Power PHEMT MMIC(gray) compared with its typical 3" counterpart (black).

Of particular note is the tight distribution across the test group. The direct similarity with the 3" V-band MMICs can be seen in these plots. The tight distribution is a result of the excellent material quality and improved manufacturability, made possible by utilizing the 6" foundry line. Figure 4 (inset) shows the layout of the balanced V-band MMIC amplifier. It is balanced to avoid phase imbalance problems associated with large gate peripheries at high frequency. The total gate periphery of the output stage is 1.6 mm, based on eight cells each containing 4x50µm gates. The die size is 3.4 x 3.6 mm (12.24 mm^2).

RELIABILITY OF PHEMT MMIC

High temperature tests have been performed on V-band dual-stage full power MMICs. During the RF reliability test, the MMIC was biased at Vds=4.5V under 4.5dB compression. Fig. 6 shows the MMIC high temperature power stability over 240 hours. It is important to note that the average power deviation was only -0.1dB and leveled off within 40hours. Thermal modeling based on device type and test condition was used to calculate channel temperature during testing, using the base plate temperature. During the testing, channel temperature was 175˚C.

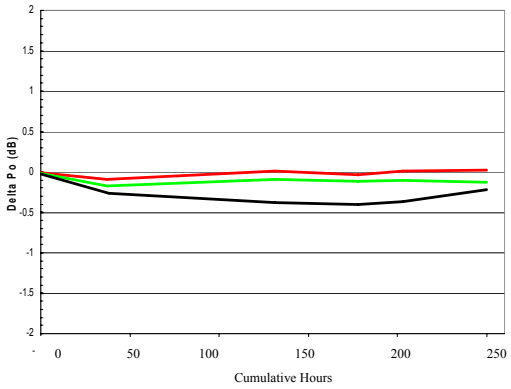

Fig.6.: Measured saturated power change during high temperature RF testing. $T_{baseplate}$ = 125˚C, Tch=175C, Compression=4.5dB

CONCLUSIONS

In this paper, we have demonstrated the world's first 0.1µm 6" PHEMT MMIC process on 2-mil substrates with excellent line yield and uniformity. Using this technology we have shown statistical DC and RF performance at V-band in comparison with its mature 3" counterpart. High temperature reliability testing performed on the V-band circuit indicates negligible power change, proving the robustness of this process. We attribute the excellent performance to epi-

design, MMIC design, and excellent processing techniques employed on our 6" PHEMT line.

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