Development of AlGaN/GaN High Power and High Frequency HFETs under NEDO's Japanese National Project

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Abstract

NEDO's Japanese national project on high power and high frequency nitride device is overviewed. Studies on correlation between crystal defects and device performances, electric field and thermal distribution in the device under operating conditions are demonstrated. Excellent CW RF output power of 230 W from a single chip and 371 W peak saturation power from an amplifier composed of paralleled HFET die are achieved at 2 GHz from Recessed FP gate structure. With a development of dual FP gate HFET, a state-of-the-art combination of 160 W output power and a 17.5 linear gain are realized at 2 GHz. At 30 GHz, 5.8 W CW operation are observed from T-gate HFET.

INTRODUCTION

Wireless communication network is one of the most important infrastructure of 21 century ubiquitous IT society. Next generation wireless communication system enabling mobile and broad band communication requires development of advanced high frequency electronic devices with high power, high efficiency and good linearity.

On the other hand, nitride electronic devices, especially AlGaN/GaN HFETs, are attracting increasing attentions recently because of its very high voltage and high frequency operations.

Remarkable progress in high power operation over 100 W at 2 GHz [1-5] and over 3 W at 30 GHz [6-8] were reported very recently using AlGaN/GaN HFET.

Recognizing such very high potential of AlGaN/GaN HFETs for high power and high frequency applications, NEDO started to support development of AlGaN/GaN HFET as "Regional Consortium Project on Development of Nitride Semiconductor Electronic Devices for Mobile Communication and Sensors" from May, 1999 through March, 2002. Pulsed operation with 113 W output power from AlGaN/GaN HFETs on thinned sapphire substrates were achieve in this project [9].

Following this NEDO's regional consortium project, bigger national project on high power and high frequency nitride semiconductor devices has started from Sep., 2002 as 5 year project. In this paper, overview on NEDO's project shall be given with some of our recent results on device and material characterization, proposed new device structure, as well as high power and high frequency performances of developed devices.

OVERVIEW OF NEDO'S NATIONAL PROJECT

The fund from METI to FED and AIST on this project comes through NEDO. Here, FED is a foundation established by the Japanese electronics industries in 1981 under the license of MITI. Research and development of this device is carried out at "Advanced High Frequency Device R&D Center in FED". Ritsumeikan University from academic sector, AIST from government and NEC and Toyoda Gosei corporations from device and material companies have participated as main players of this project.

NEC and Toyoda Gosei have indicated their interests in developing device and material technologies and expressed their strong intension to transfer developed technologies in this project to production level after finishing of this project. Other companies, Furukawa Electric, Oki Electric, Mitsubishi Electric, Hitachi Cable, Matsushita Electric, Sumitomo Electric, and ULVAC, on the other hand, are interested in more fundamental research subjects closely related to this device development.

Figure 1 summarizes the structure, responsible fields, and participating members of each site. Ohtsu site, where NEC is

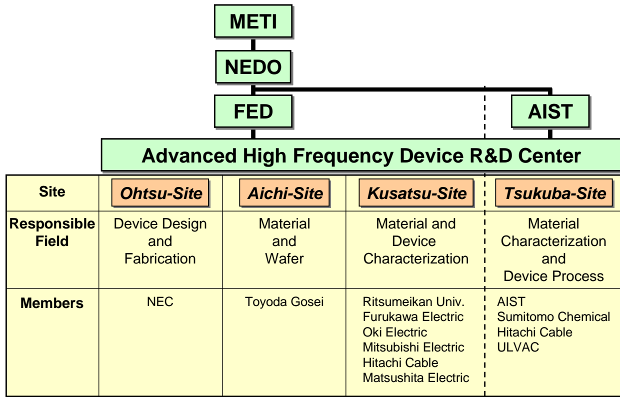

Fig. 1 High-power and high frequency nitride semiconductor device project (2002.9~2007.3).

located, is responsible for 2 GHz, 5 GHz, and 26 GHz device design, and related device fabrication technologies. Aichi site, where Toyoda Gosei is located, is responsible for material and wafer technologies, including 2-inch and 4-inch MOCVD epitaxial growth of hetero-structure. At Kusatsu site, located on the campus of Ritsumeikan University, Ritsumeikan University and five companies are collaborating each other to carry out material and device characterization works, correlating materials properties and actual device performances. At Tsukuba site, where AIST is located, AIST and three other companies are collaborating each other in performing material characterization and developing new device processes.

Major targets of device performance for midterm review at the end of 2004 were 200 W, 100 W, and 5 W at 2 GHz, 5 GHz, and 26 GHz, respectively, whereas those for final term review at the end of 2006 are 200 W and 20 W RF output power at 5 GHz and 26 GHz, respectively.

WAFER AND DEVICE CHARACTERIZATION

Effects of defects in substrate material both on hetero-structure epi-layers and on fabricated HFET device performances are major concerns for most of the device engineers in this field. Observing electric field and temperature distributions in the device under operating conditions are also another big interests. Such kind of characterization works are carried out mainly at Kusatsu and Tsukuba sites.

To clarify the effects of micro pipes in SiC substrates on device performances, HFETs were fabricated carefully on and around hollow core of micro pipes with precise positioning. Poorer pinch off characteristics and larger leakage current were clearly observed, when the devices were located closer to the hollow core within the distance of 40 μm [10].

Raman spectroscopy revealed that the density of free carriers in GaN increased near the hollow core of the micro pipe.

A localized intensive electric field between gate and drain contacts is considered to be one of the major origins of premature breakdown. Direct observation of electric field in the actual devices under operating condition is very attractive for further improvement of device performances and reliability. Such electrical field characterization has been carried out by using KFM.

Figure 2 shows how potential distribution in the cross section of a cleaved HFET changes as gate bias voltage becomes deeper from -2 V to -10 V. Electric field is found to concentrate in the regions between gate and drain as well as around the buffer layer between GaN and SiC.

The V_{DS} dependence of the electric fields has also been studied till the device eventually breaks down at V_{DS} = 40 V (V_G = -10 V). Electric fields, however, increased almost in proportion to V_{DS} without any extraordinary phenomena predicting breakdown.

Temperature distribution observation of AlGaN/GaN HFET under operating condition is an another attractive subject for the development of high power and high reliability device. A micro-Raman spectroscopy has been used for this purpose. Argon laser (514.5 nm) with spatial resolution of around 1 μm was used as a laser source. Temperature of the device was estimated from Raman shift of E_2 phonon mode. Figure 3 shows observed temperature distribution of a typical HFET on sapphire driven by an electric powers of approximately 480 mW (V_{DS} = 40 V, V_G = 1.0 V, 12 W/mm).

A high temperature region of around 290 °C, which seems to correspond to a high electric field region, appears at the gate edge facing the drain contacts.

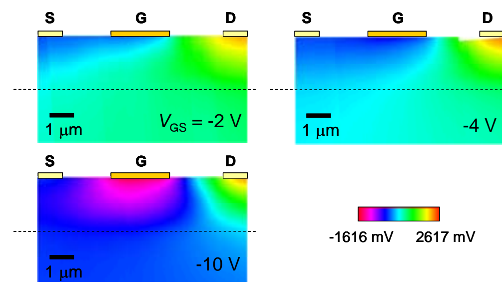

Fig. 2 Potential distribution in the cross section of a cleaved HFET.

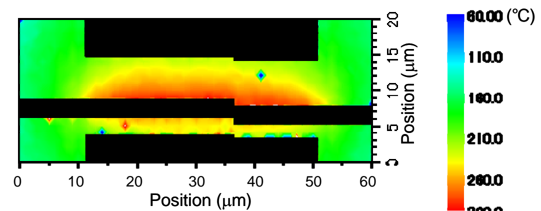

Fig. 3 Temperature distribution of AlGaN/GaN HFET on sapphire at V_{DS} = 40 V and V_G = + 1 V (gate length 3 μm, gate width 40 μm, source-gate spacing 2 μm, gate-drain spacing 5 μm).

DEVICE STRUCTURE AND PERFORMANCES

It is widely recognized that power performance of AlGaN/GaN HFET is limited by an undesirable effect of current collapse induced by electron trapping at the surface states. SiN passivation film on AlGaN top layer decreases this current collapse. However, trade off relation between current collapse and breakdown voltage have become apparent.

To improve this trade off relation, a recessed gate FET with a field modulating plate (FP) [3, 11], as shown in Fig. 4 (a), has been developed. Using this device structure, suppression of collapse, high voltage operation and improved gain performance have been successfully realized simultaneously. FP electrode is found to be very effective in suppressing major part of current collapse [12, 13], whereas additional gate recess is effective to further minimize the residual current collapse as well as to increase breakdown voltage with reduced gate leakage current [3, 11, 14]. The gate-drain breakdown voltage defined at 1 mA/mm was improved from 160 V to 200 V after applying recessed structure to planar FP structure [13].

Corresponding to the adoption of FP gate structure [12, 13] and additional recessed gate FP structure [3, 11, 14], rapid progress has been made in total output power from a single chip HFET within a relatively short period of time. Figure 5 demonstrates rapid annual progress of L-band AlGaN/GaN HFETs in terms of total output power from a single chip.

Figure 6 shows output power, linear gain and power-added efficiency for 48 mm-wide FP-FET as a function of input power at a drain-bias voltage of 53 V.

Based on this recessed gate FP structure, a single-ended amplifier using a 48 mm-gate width single-die GaN-HFET was developed for CDMA cellular base-station systems. The developed amplifier delivered a peak saturation power of 280 W with a linear gain of 12.6 [15].

The amplifier composed of paralleled 48 mm gate width HFET die was also developed recently. This amplifier delivered a peak saturated output power of 371 W with a linear gain of 11.2 dB at a drain voltage of 45 V under 2.14 GHz 3 GPP W-CDMA signal output, as shown in Fig. 7. A low 5 MHz-offset ACLR of -36 dBc with a drain efficiency of 24 % is also obtained at 8 dB power back off from the saturated output power [16].

A C-band compact amplifier was also successfully developed. The developed amplifier with a single chip 24 mm-wide recessed FP-FET delivered a 61 W (2.5W/mm) output power with 10.2 dB linear gain and 42 % power added efficiency under CW operating conditions [17].

At Ka-band, 0.25 μm T-shaped gate device was developed by using process combining electron-beam and i-line lithography. To achieve high output power with a one cell type FET, a combination of unit gate-finger length and a total gate width were carefully investigated [18]. Saturated power of 5.8 W with a linear gain of 9.2 dB and a power added efficiency of 43.2 % have been successfully achieved at 30 GHz. Output power, power gain, and a PAE at 30 GHz from this 1.0 mm wide device as a function of input power is shown in Fig. 8 [18].

Serious problem related to a trade off relation between current collapse and breakdown characteristic has been much improved by applying FP structure. In this structure, however, gain is slightly reduced by the increase in gate-

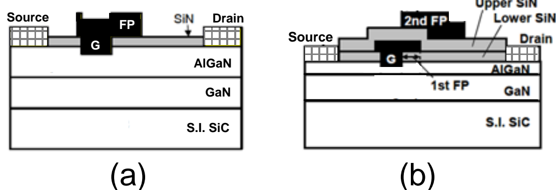

Fig. 4 Schematic of recessed gate structure: (a) FP FET and (b) dual-FP FET.

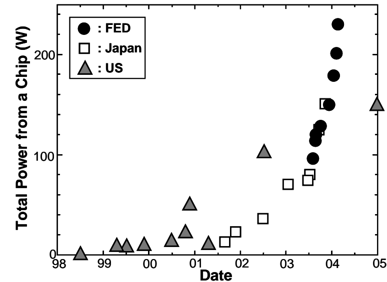

Fig. 5 Annual progress of L-band AlGaN/GaN FETs in terms of total output power from a single chip.

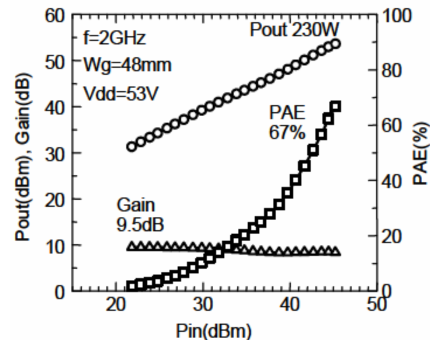

Fig. 6 Output power, linear gain and power-added efficiency for 48 mm-wide FP-FET as a function of input power.

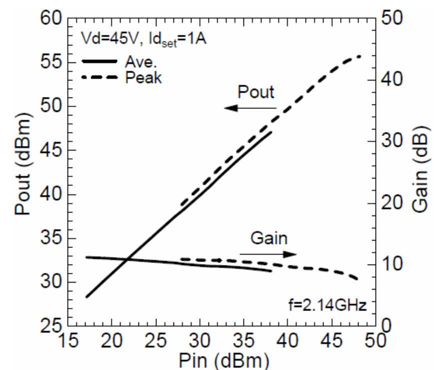

Fig. 7 Output power and linear gain from the amplifier composed of paralleled 48 mm gate width HFET die.

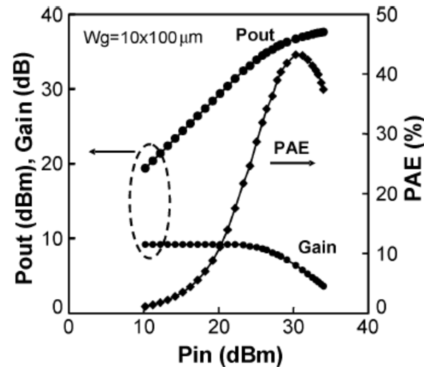

Fig. 8 Output power, power gain, and PAE at 30 GHz from a 0.25 μm T-shaped gate FET.

drain capacitance. Dual field-modulation plate structure with additional source-terminated FP as shown in Fig. 4 (b) has been developed to reduce gate-drain capacitance [19].

Owing to reduction in feed back capacitance, this device provided 3-dB higher gain along with increased linear gain. The breakdown voltage is also increased from 125 V to 250 V by applying this second FP.

Under a 2.15 GHz W-CDMA modulation scheme, a dual-FP-FET with a 24 mm gate periphery achieved a state-of-the-art combination of 160 W output power and a 17.5 dB linear gain.

CONCLUSIONS

NEDO's national project in Japan on high power and high frequency nitride electronic devices is overviewed. As for the basic research, influence of defects in SiC substrates on FET performances, electric field and thermal distribution in the operating devices are intensively studied by using Kelvin prove method and micro Raman spectroscopy.

Recessed HFETs with a FP gate have been developed. A single chip device has demonstrated excellent HF power performances of 230 W CW operation at 2 GHz and a 156 W pulsed operation at 4 GHz. An amplifier composed of paralleled 48 mm gate periphery FET die delivered a peak saturation power of 371 W with a linear gain of 11.2 dB under 2.14 GHz W-CDMA signal output, demonstrating excellent feasibility for application to cellular phone base station.

HFET with dual FP have recently been developed. 24 mm gate periphery device demonstrated a state-of-the-art combination of 160 W output power and a 17.5 dB linear gain under 2.15 GHz W-CDMA signal modulation scheme.

T-shaped 0.25 μm gate HFET showed 5.8 W CW output power at 30 GHz.

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ACRONYMS

NEDO: New Energy and Industrial Science Development Organization
METI: Ministry of Economy, Trade and Industry
FED: R&D Association for Future Electron Devices
AIST: National Institute of Advanced Industrial Science and Technology
HFET: Hetero-structure Field Effect Transistor
FP FET: Field Modulating Gate FET
KFM: Kelvin Force Microscope
ACLR: Adjacent Channel Leakage Power Ratio