Recent Achievements in SopSiC substrates for High Power and High Frequency Applications

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Abstract

Engineered Substrates is an established material in the silicon industry. Engineered substrates enable the optimization of the active device, the top layer and the bulk independently. Today we present the development of Silicon silicon on poly-crystalline Silicon silicon Carbide carbide (SopSiC) substrate obtained by the Smart Cut™ technology. SopSiC substrate structure combines the advantages of Silicon and SiC materials. Compared to the conventional SiC single crystal approach, this innovative approach offers a larger diameter substrate and a lower cost solution. SopSiC substrates are proposed to support the development and future industrialization of GaN microelectronics for commercial and military applications. The recent results, presented hereafter, show that materials could cover various areas from high frequency to high power devices such as AlGaN/GaN transistors.

I-PROCESS

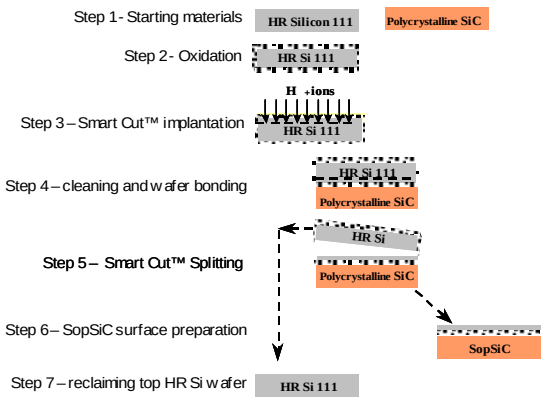
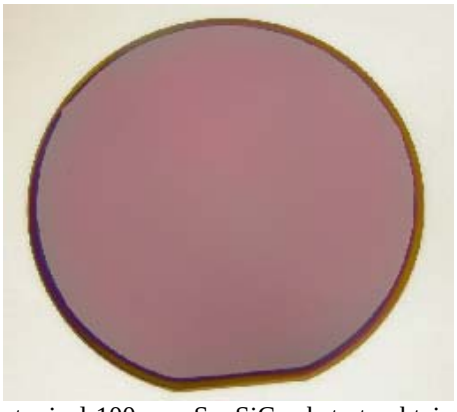


Figure 1: process flow applied to SopSiC substrate realization

The SopSiC process flow differs slightly from the SOI process flow (UNIBOND™), since the base substrate is a polycrystalline cubic SiC substrate (poly SiC) instead of a silicon substrate. Figure 1 summarizes this process flow. The starting materials are a high resistivity (111) silicon wafer (HR Si) and a polycrystalline cubic SiC substrate. Both are available in different sizes, from 2 inches to 12 inches. The poly-SiC substrate is highly resistive (10^5 Ω·cm) and has thermo-mechanical characteristics close to the single crystal SiC as described in the introduction. The used silicon substrate is also highly resistive (above 10^4 Ω·cm). We will show in the next paragraph that the electrical characteristics of this substrate are not altered by the Smart Cut™ technology.

The typical process flow is thermal oxidation and hydrogen implantation of the HR Si substrate, surface preparation and room temperature wafer bonding between HR Si and poly SiC substrates. After wafer bonding, the Si film is splitted, resulting in a SopSiC substrate. Additional treatments follow to stabilize the structure and prepare the silicon surface of SopSiC to be epi-ready for the subsequent III-Nitride epitaxy. Typical parameters are close to standard UNIBOND SOI: hydrogen implanted dose is typically between $4 \cdot 10^{16}$ and $7 \cdot 10^{16}$ $H^+ \cdot cm^{-2}$ and implantation energies from 50 to 200 keV. Picture 1 shows a 100 mm epi-ready SopSiC substrate.



Picture 1: typical 100 mm SopSiC substrate obtained by the Smart Cut™ technology As observed in this picture, an excellent layer transfer quality is obtained showing no large macroscopic bonding defects

II- PERFORMANCES

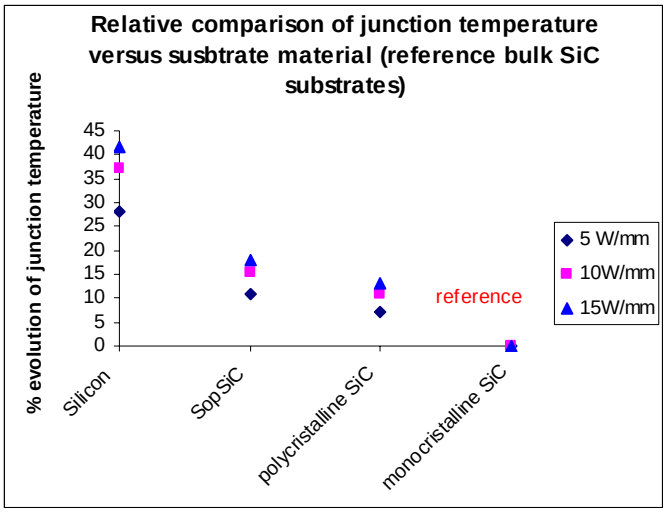


Figure 2 : maximal computed junction temperature as a function of the substrate nature. The comparison is drawn for a range of power density to be dissipated from 5 to 15W/mm.

Thermal simulation and RF probe measurement have been performed. Finite Element numerical calculations were used to predict and compare the maximum gate temperatures for various substrates under the GaN layer on a simple 2D structure. The applied boundary conditions were heat fluxes on the channel area and a heat sink (constant temperature to 50°C) on the backside of the structure to represent the device cooling. 3 levels of heat fluxes were studied, corresponding to 3 levels of power density 5, 10 and 15 W/mm to be dissipated and thus representing CW working conditions of high frequency devices (W/mm refers to electrical energy dissipated per gate length development).

The SopSiC is expected to show thermal capabilities close to those of polycrystalline SiC. Compared to bulk silicon, this engineered substrate exhibits a major improvement in terms of heat dissipation.

Another step was to verify the electrical properties of the poly-SiC. The RF losses become very critical as the frequency increases up to the millimeter wave applications. So 50 Ohm coplanar transmission lines have been processed on a poly-SiC substrate to determine the RF losses. No process via has been used. By using the standard S parameters characterization, the attenuation factor has been extracted from 2 transmission lines of 2 and 3 mm. In addition, this study has been extended by measuring the RF losses at different temperature in a range from 25 ºC up to 200 ºC.

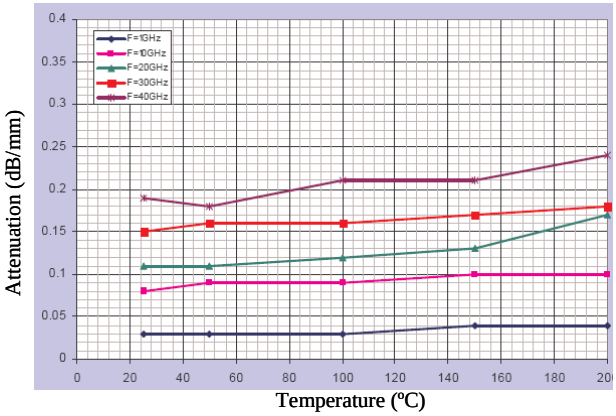


Figure 3: Characterization of RF losses in the poly-SiC substrates vs. temperature and frequency

The performances, presented in Figure 3, remain unchanged regarding the temperature. Also, the poly-SiC behaves as good as the GaAs substrate for the microwave and millimeter wave frequencies.

III- CONCLUSION

The exposed results prove that the SopSiC has excellent electrical and thermal properties. Besides, SopsiC substrates are fully compatible with the compounds semiconductor device manufacturing. SopSiC material is the solution to bring low cost approach and high performances necessary for high power and high frequency devices.