SiN Capacitors and ESD

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Abstract

We present Human Body Model (HBM) electrostatic discharge (ESD) test results for the three types of capacitors used in the TriQuint Texas high density interconnect process. We show a linear dependence of ESD failure voltage with respect to capacitor area (capacitance). We also show doubling of the HBM failure voltage when using two capacitors in series compared to a single capacitor of the same type with the same total capacitance. Surprisingly high HBM failure voltages were observed for large 500 Å SiN capacitors. Transient simulations were performed to relate the observed HBM failure voltages to the intrinsic dielectric breakdown voltages of the three types of capacitors. By incorporating a dielectric current leakage due to Frenkel-Poole emission from traps into the simulations, we were able to obtain an excellent agreement with the HBM test results.

INTRODUCTION

In recent years, there has been a significant increase in interest among the GaAs manufacturers towards ESD circuit protection. The continuous trend of decreasing die size has had a negative effect on circuit ESD robustness. Manufacturers have found that scaling FET channel geometries down to achieve higher frequency performance, using thinner dielectrics to achieve higher capacitance densities, and placing components closer together to optimize substrate usage, have had an adverse effect on the GaAs circuit ESD sensitivity. At the same time, commercial applications are posing to the GaAs manufacturer ESD sensitivity requirements similar to those achieved by silicon manufacturers. Compliance with such requirements often can only be achieved after careful layout consideration and the addition of special ESD protection structures into the circuit under consideration. In order to enable the designer to make an educated choice from different process and layout options for increased ESD robustness, the individual effects of using these different options need to be studied and well understood. For this reason, we conducted an extensive HBM characterization of components from the most widely used TriQuint Texas processes including FETs, diodes, capacitors, resistors, and isolated gaps between different metal interconnects. Results of this study from various structures were reported in [1]. The purpose of this paper is to report some very interesting capacitor ESD stress results and to provide an explanation of the peculiar findings.

HBM CAPACITOR TEST RESULTS

MIM structures with a large range of capacitances and serving different purposes (bypassing, matching, DC blocking) are employed in most microwave circuits. Matching and DC blocking capacitors are particularly vulnerable to ESD damage due to the fact that they are generally small and are often located directly at the circuit input or output, making them the first components in the ESD transient path. Therefore, a capacitor ESD sensitivity assessment was one of our major tasks.

The capacitor characterization project involved testing several different sizes of the three silicon nitride capacitor types currently used in our high density interconnect process. The fabrication sequence for these capacitors is described in [1]. Their dielectric thickness and capacitance density are as follows: 500 Å (1200 pF/mm^2), 2000 Å (300 pF/mm^2), and 2500 Å (240 pF/mm^2). A list of capacitor sizes tested is presented in Table 1, while the results of our testing are plotted in Figure 1.

TABLE 1
LIST OF CAPACITORS TESTED

Dielectric Thickness (Å)	Capacitance Density (pF/mm^2)	Cap Size X (μm)	Cap Size Y (μm)	Capacitance (pF)
500	1200	4	4	0.0192
500	1200	20.4	20.4	0.50
500	1200	50	50	3.00
500	1200	91.25	91.25	9.99
500	1200	123	78	11.51
2 x 500	600	28.85	28.9	0.50
2 x 500	600	64.5	64.5	2.50
2 x 500	600	111.8	111.8	7.49
2000	300	4	4	0.0048
2000	300	122	77	2.82
2500	240	4	4	0.00384
2500	240	123	78	2.30

During our tests, we found as expected, that for small capacitor sizes thicker dielectric resulted in higher HBM failure voltages. However, we were very surprised to discover that for large capacitances, the capacitors with thinnest

dielectric sustained the highest HBM voltages prior to failure. This effect is pronounced even more strongly when failure voltages are compared for the same capacitor area. For instance, the 500 Å capacitors of area 9594 μm^2 have 2.4 and 3.6 higher magnitude failure voltages for positive and negative polarity transients, respectively, compared to the 2500 Å capacitors with the same area. This result was considered counterintuitive at first and required further investigation. A transient simulation was performed, the results of which are discussed later in this text.

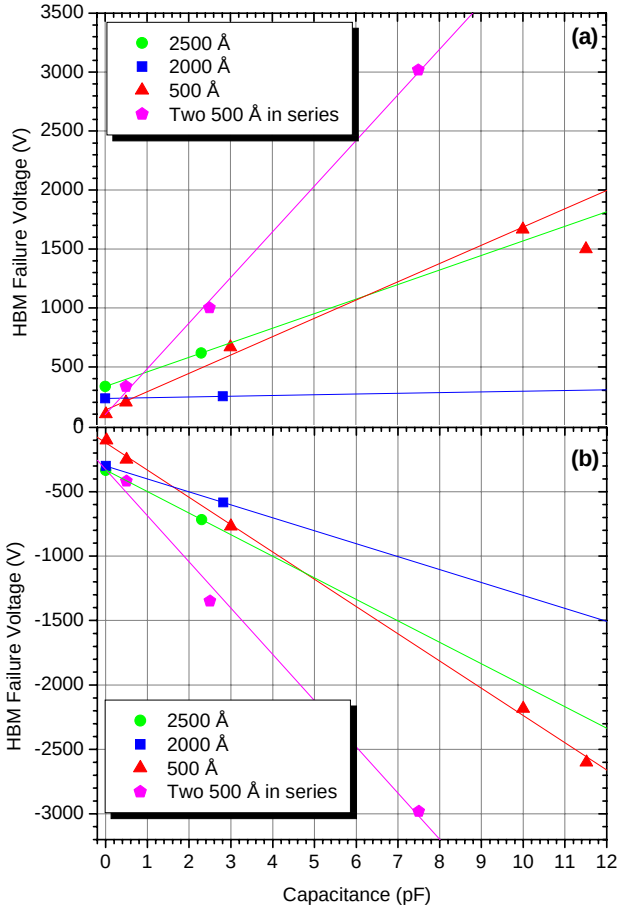

Fig. 1. Human Body Model ESD failure voltages for three different dielectric thickness capacitors: (a) Positive transients; (b) Negative transients.

In addition, we found a linear dependence of failure voltage with capacitance (capacitor area) and a doubling of the failure voltage when substituting a single capacitor with two larger capacitors of the same type and the same total capacitance bonded in series. Although these two results were shown for the 500 Å capacitors only, they are expected to apply for all capacitor types and can be used by the circuit designer in order to boost the circuit ESD robustness.

We also discovered a voltage polarity dependence, similar to the one previously seen in capacitor ramped and fixed voltage tests [2, 3]. We recorded slightly higher failure voltage magnitudes for negative polarity HBM transients compared to positive transients. Even though this result cannot be directly employed in increasing the ESD circuit robustness because the polarity of the incoming ESD transient is unknown and can vary, this was still an interesting finding showing the consistent capacitor behavior under both DC and transient stress conditions.

Discussion

In the absence of processing defects, capacitors fail when the intrinsic breakdown voltage of their dielectric is exceeded. In this context, "breakdown" refers to the catastrophic failure of the dielectric. The intrinsic breakdown voltage is a function of the properties of the SiN film and it scales linearly with the film thickness. Some lot-to-lot variation is present due to small differences in the nitride properties and thickness. In general, however, through ramped voltage tests (0.4 V/s - 4.0 V/s) we have observed that our capacitors have the following breakdown voltages: 35-45 V for 500 Å, 130-160 V for 2000 Å, and 170-200 V for 2500 Å capacitors. Similar failure voltages have been observed during transmission line pulse (TLP) testing in short-pulse test conditions similar to those seen during HBM transients (Figure 2). The intrinsic breakdown voltages are significantly lower than the HBM failure voltages observed, suggesting that a voltage clamping must be occurring during the HBM tests. Also, it was unclear why the capacitor HBM failure voltages would depend on capacitor size and, furthermore, why a 500 Å capacitor would sustain much higher HBM voltages than the same area capacitors with 4 or 5 times thicker dielectrics.

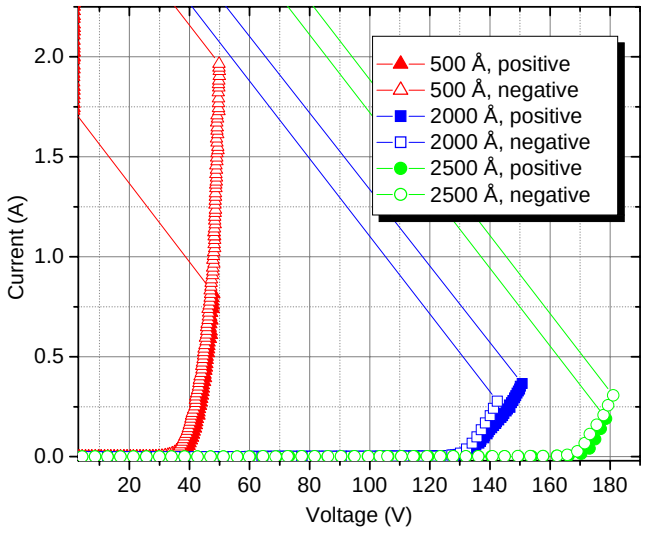

Fig. 2. TLP failure voltages for three different dielectric thickness capacitors, both positive and negative transients.

Transient Simulations

In order to investigate the unexpected HBM results, transient simulations were performed for different capacitor types and sizes using Advanced Design System (ADS). The

standard HBM equivalent circuit with a 100 pF shunt capacitor and a 1.5 kΩ series resistor (Figure 3) was used. Initially, we obtained very little reduction of voltage at the capacitor under test (Figure 4). The voltage reduction was due to charge redistribution between the capacitor under test and the human body model capacitor with an equilibrium voltage given by the simple expression $V = V_{HBM} C_{HBM} / (C + C_{HBM})$, where V_{HBM} is the transient pulse voltage, C_{HBM} = 100 pF, and C is the capacitance of the device under test. This slight voltage reduction was clearly not sufficient to explain our HBM test results and we needed to search for a different explanation.

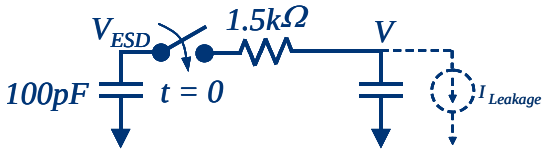

Fig. 3. HBM equivalent circuit schematic. A current source has been added to represent the capacitor dielectric leakage.

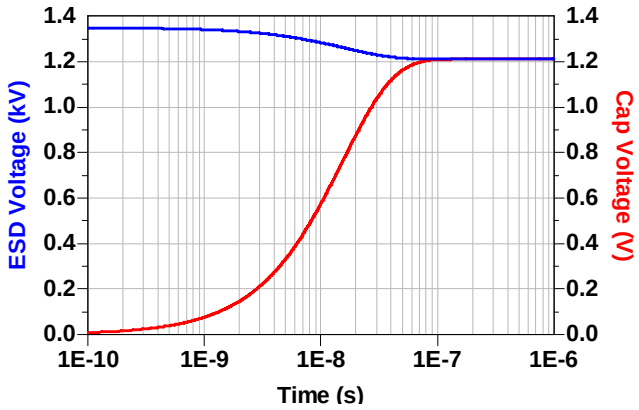

Fig. 4. HBM transient simulation time response plot for the largest size 500 Å capacitor tested. 10 % reduction of voltage was observed on the capacitor under test due to charge redistribution. This voltage reduction is insufficient to explain the HBM test results. The voltage reduction for all other capacitors tested would be even less due to their smaller capacitance values.

Next, we considered a leakage path through the capacitor dielectric, which would provide means for safely dissipating the ESD charge without catastrophic failure. The leakage current (Eqn. 1) is due to Frenkel-Poole emission from traps [4, 5]. It is voltage dependent and is directly proportional to capacitor size, which explains the HBM failure voltage linear dependence of capacitance (capacitor area). It is also dependent of dielectric thickness and the leakage current through the 500 Å capacitors is higher compared to the other capacitor types biased at the same voltage. This explains why large 500 Å capacitors are able to sustain higher HMB transients compared to similarly sized capacitors with thicker dielectric.

$$J = C_1 E e^{-q(\phi_B - \sqrt{qE/\pi\varepsilon_i})/kT} = \frac{C_1 V}{d} e^{-q(\phi_B - \sqrt{qV/\pi\varepsilon_i d})/kT} \quad (1)$$

where J is the current density, C_1 is a constant, E is the electric field, V is the applied voltage, T is the temperature, ϕ_B is the barrier height of the traps, d is the capacitor dielectric thickness, $\varepsilon_i = \varepsilon_0 \varepsilon_r$ is the dielectric constant, q is the charge of the electron, and k is Boltzmann's constant.

Typical leakage currents for different capacitor types and sizes are presented in Figure 5. All data correlates well with the Frenkel-Poole conduction model. The measured leakage currents were used to extract the constants of interest in Eqn. 1. A voltage dependent current source utilizing Eqn. 1 was then added to the HBM schematic to account for capacitor leakage current during the ESD event.

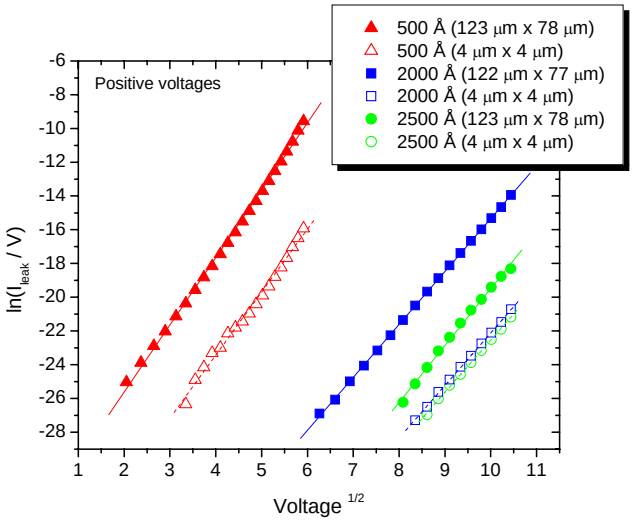

Fig. 5. Frenkel-Poole fits to current leakage data collected from small and large capacitors of all three types.

In result of the leakage current source added, the voltage on the capacitor during simulation was clamped down to a significantly lower value than the HBM transient voltage. This effect was most dramatic for the largest size 500 Å capacitor which allowed the highest amount of dielectric leakage (Figure 6). In all simulations, we achieved a good agreement between the transient failure voltage of the device under test and the previously known voltages corresponding to the intrinsic dielectric breakdown for each capacitor type. The results are shown in Table 2. Some of the simulated failure voltages exceed slightly the intrinsic breakdown voltages. We believe this is due to the 50 V minimum step of our test system limiting the accuracy of the transient failure voltage determination. Since the transient failure voltages for the small capacitor sizes are generally small, the relative error for those capacitors is larger resulting in a larger overestimate of failing voltages compared to the large capacitors.

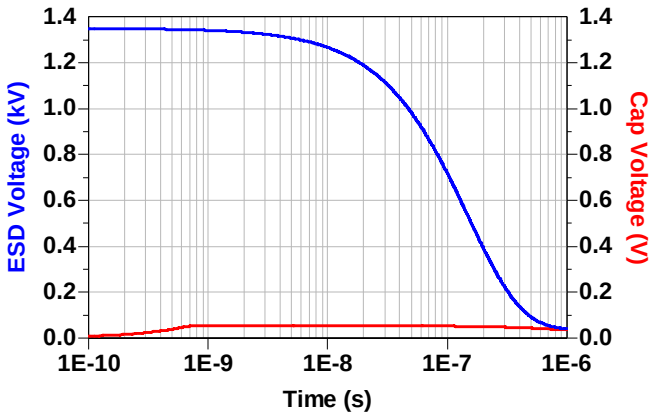

Fig. 6. HBM transient simulation time response plot for the largest size 500 Å capacitor tested with included parallel current source representing the dielectric leakage path due to Frenkel-Poole emission from traps. The voltage on the capacitor under test is reduced to a value close to its intrinsic breakdown voltage.

TABLE 2
COMPARISON OF MEASURED HBM TRANSIENT VOLTAGES, CALCULATED CAPACITOR VOLTAGES AFTER TAKING INTO ACCOUNT CHARGE REDISTRIBUTION, AND SIMULATED CAPACITOR VOLTAGES, BOTH WITH AND WITHOUT LEAKAGE CURRENT.

Capacitor Dielectric Thickness (Å)	Cap Size X (μm)	Cap Size Y (μm)	Capacitance (pF)	Measured HBM Transient Failure Voltage (V)	Voltage on DUT Calculated from Charge Redistribution (V)	Voltage on DUT from HBM Simulation, NO LEAKAGE (V)	Voltage on DUT from HBM Simulation, WITH LEAKAGE (V)
500	4	4	0.0192	100	100	100	66
500	123	78	11.51	1500	1345	1344	55
2000	4	4	0.0048	200	200	200	190
2000	122	77	2.82	250	243	243	153
2500	4	4	0.00384	333	333	333	217
2500	123	78	2.30	617	603	603	191

CONCLUSIONS

An ESD study was conducted in order to assess the robustness of our capacitors and to provide means for the circuit designer to select capacitor components with greater ESD robustness. We observed linear dependence of human body model failure voltage as a function of capacitor area (capacitance). We also observed that large capacitors with thinner dielectric could sustain higher human body model stresses than capacitors of the same area and a thicker dielectric. Both of these results were correlated to increased dielectric leakage, which allowed for safely dissipating the charge in the ESD transient. Our findings were investigated via transient simulations incorporating a voltage dependent capacitor dielectric leakage. These simulations predicted a significant voltage reduction at the capacitor under test. The voltages simulated in this manner are in good agreement with the intrinsic capacitor breakdown voltage characteristics of each capacitor type. This simulation method can be used by designers for evaluating the ESD hardness of capacitors. A similar approach based on current and voltage device handling limitations and specific I-V characteristics could be expanded into simulating other circuit components as well.

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