The Reliability Study of MIM Capacitor Built On Top of Backside Via In III-V Compound MMIC

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Keywords: MIMCAP; Through-Substrate Via; Breakdown; Thermal Cycles; Failure Rate

Abstract

We report a compact and reliable MIMCAP directly on backside through via (MIMCAP-On-Via). The potential performance effects of a capacitor on backside via is explored with changing via density and the total number of vias. The MIMCAP-On-Via reliability was verified using a time dependant dielectric breakdown mode, and its reliability is comparable to a conventional MIMCAP. The thermal stability of epoxy mounted MIMCAP-On-Via test structures was also verified over the -55˚C to 125˚C temperature range with no failures.

INTRODUCTION

As III-V compound technologies evolve, and further demand is being pressed upon the functionality and manufacturing cost of MMICs, there is an increasing need to reduce chip area through circuit compaction. One of the initiatives for this compaction campaign is to directly connect the through-substrate via underneath a MIMCAP on the front side, so that the traditional interconnect metal pad solely used for through-substrate via connection can be eliminated from the layout.

Since MIMCAPs have been widely used in the semiconductor industry as an important passive circuit component, reliability models have been extensively studied. However, few studies or existing capacitor reliability models contain backside through-substrate via underneath the MIMCAP [1]. This study is to fabricate MIMCAP residing on top of the through-substrate via, explore the potential effect of via on capacitor electrical, mechanical and thermal performance, and conduct dielectric and thermal reliability study in comparison to the conventional MIMCAP.

MIMCAP-ON-VIA FABRICATION

Fig 1 illustrates a cross section of a fully fabricated MIMCAP atop a backside via. The MIMCAP top and bottom metal plates are constructed differently depending on the process flow of the transistor process design, but they both use electron beam evaporation for the deposited metals. The MIM nitride is formed by PECVD deposited silicon nitride (SiNx) at 250°C with nominal refractive index 2.0, thickness 1000Å, and tensile stress 250MPa. This capacitor has a nominal 600pF/mm^2 sheet capacitance

EXPERIMENT DESIGN AND TEST SETUP

The existence of a via underneath a capacitor, as illustrated in Figure 1, poses a potential mechanical and electrical reliabiltiy risk. More specifically, the via may be regarded as an external defect that could eventually degrade capacitor performance or reliability. This study attemps to statistically study the deleterious effects of two designated parameters to represent the defect distribution. One parameter is the total number of vias within a capacitor, while the other is the spacing between vias. Figure 2 shows a schematic of the via layout design for a given capacitor area. There are two series of variables ("x' and "y") incorporated in the design of experiment. One series, x, keeps the total number of via at 35 at each spacing while the via spacing increase from 60um, 90um to 120um, while the other series, y, spreads the vias over the whole area of capacitor without limitation on the total number of via at each spacing. At the same time, a capacitor without vias is used as a control part.

To determine how the MIMCAP-On-Via fares during the process flow of transistor wafer fabrication and ensuing chip mounting and thermal cycles, four test stages are set up as configured in Figure 3 to track the capacitor performance by conducting visual inspection and ramped voltage breakdown test at each stage. For ramped voltage breakdown test, the voltage ramp-up rate is set at 50V/sec with 2.0mA current and 200V in compliance. For thermal stability test, the wafer is diced into chips. All chips are epoxy-mounted on metal plates. Thermal cycles are conducted in the temperature range from -55°C to 125°C for 10 cycles

RESULTS

Figure 4a and 4b show the capacitor breakdown performance after backside vias are fabricated for "x" and

"y" series respectively. The via density or the total number of vias do not have any effect on the ramped voltage breakdown of the capacitor. Most specifically, the MIMCAP-on-Via demonstrates better ramped voltage breakdown characteristics as compared to the control capacitor. All four test stages show there are no deleterious effects of vias underneath a capacitor.

Since there is no difference on breakdown probability among all x and y series at each test stage, Figure 5 combines all x and y series into one group at each test stage, and plots them together into one chart to seek if there is any detectable trend of breakdown performance throughout the process. The resulting plot shows there is no indication of degradation for MIMCAP-On-Via going through backside process, dicing/chip picking, chip mounting and thermal cycles. Visual inspection at each test stage also shows no mechanical defects are incurred during the fabrication processes, and the MIMCAP-On-Via structures survive the epoxy mounting process and subsequent thermal cycling. Since the ramped voltage breakdown test is destructive, a different group of capacitors from the same wafer have to be allocated for breakdown test at each test station as shown in Figure 3, so the capacitors being tested at each stage may carry some natural difference, which could explain the negligible breakdown variation among those curves in Figure 5, but overall there is no meaningful trend of capacitor degradation can be established.

RELIABILITY

We use the Time-Dependent Dielectric Breakdown (TDDB) [2] to verify the reliability of the MIMCAP-On-Via. In TDDB reliability model, the nitride conduction is defined by Frenkel-Poole function that is given by (1), where J is the current density, V is the voltage applied to capacitor, d_{eff} is the effective nitride thickness. The constants are described in Table 1.

$$J = \frac{V}{d_{eff}}\left[\sigma FP * \exp\left(\frac{-\phi + \beta * \sqrt{V/d_{eff}}}{kT}\right)\right] \qquad (1)$$

Given a constant current J flowing through nitride, the time until nitride breakdown t_{BD} can be explained by (2)

$$QBD = J * t_{BD} \qquad (2)$$

By performing nitride conduction measurements at different temperatures, and charge to breakdown tests under constant current, the constants and parameters of Frenkel-Poole model can be determined. The model parameters for the MIM nitride used in this study are summarized in Table 1

A cumulative defect density, D, in a capacitor can be assessed using the Seeds yield model [3] given by (3), where P is the failure probability and A is the capacitor area. Given the breakdown probability curves at Stage D in Figure 5 and Frenkel-Poole function (1), the cumulative defect density D as a function of effective thickness can be determined, and eventually, the mission life can be predicted using the same function (3) by virtue of the defect density D for a given capacitor given the mission conditions.

$$P = 1 - \frac{1}{1 + DA} \qquad (3)$$

Figure 6 shows the capacitor mission life expectation of conventional MIMCAP and MIMCAP-On-Via at 5V operation and a mission temperature of 60°C for a capacitor of 300pF. It is clear that there is no significant difference between two types of capacitors within the accuracy of the reliability model

CONCLUSIONS

Both via spacing and the total number of via are found to have no effect on the robustness of MIMCAP-On-Via. There is no indication at all that the MIMCAP-On-Via breakdown performance suffers from the existence of underneath through-substrate via.

MIMCAP-On-Via is proven to be as reliable as the conventional MIMCAP without via. It bears the same level of failure rate as the conventional MIMCAP without via, and it can be easily integrated into the compact designs for next generation MMICs.

REFERENCES

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[2] J. Scarpulla et al, "A TDDB Model of Si3N4-based Capacitors in GaAs MMICs" The 37th Annual International Reliability Physics Symposium, San Diego, CA, p.128-137 (1999).

[3] R. Seeds, "Yield and Cost Analysis of Bipolar LSI", 1967 Int. Elect. Dev. Meeting Technical Digest, p.92

Table 1 Frenkel-poole paramenters for Mim nitride

Name	Value	Description
QBD	120 Coul/cm2	Charge to breakdown
Φ	1.06 eV	Trap level for Frenkel-Poole
σ_{FP}	1.66E-7 S/cm	Frenkel-Poole conductivity coefficient
β	4.59E-4 (cm/V)^^0.5	Frenkel-Poole emission coefficient

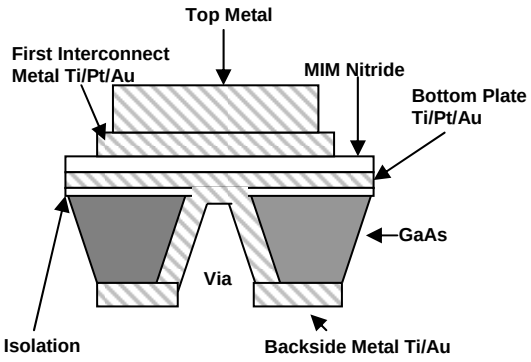

Figure 1 Cross Section of A Fully Processed MIMCAP Built On Top of Backside Via

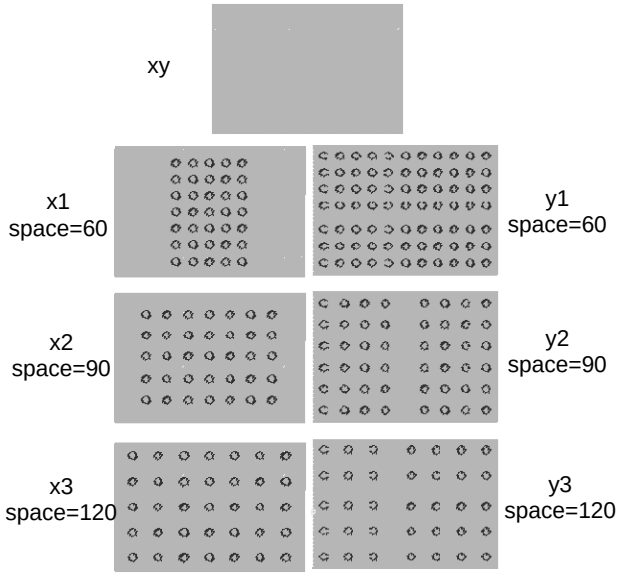

Figure 2 Backside Via Layout Pattern To Test Its Effect On Capacitor Performance

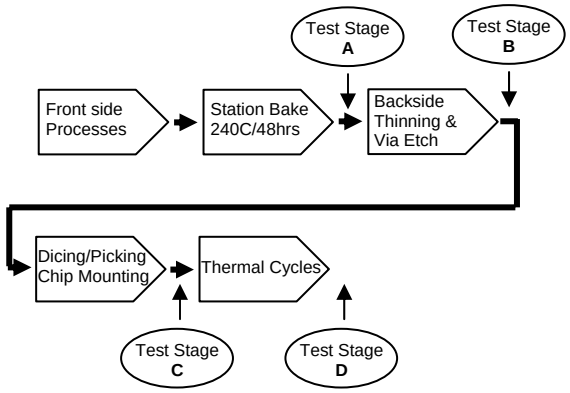

Figure 3 Fabrication Process Flow And Test Stage Setup

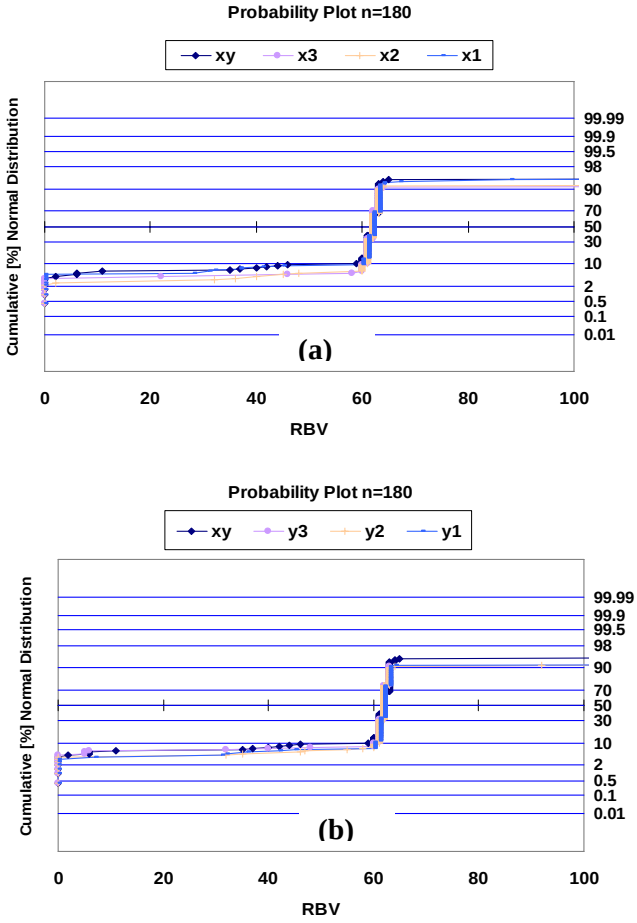

Figure 4 Capacitor Electrical Breakdown Probability Plots With Various Via Layout After Backside Process. Test Vehicle is a capacitor with area 1,057,000um2

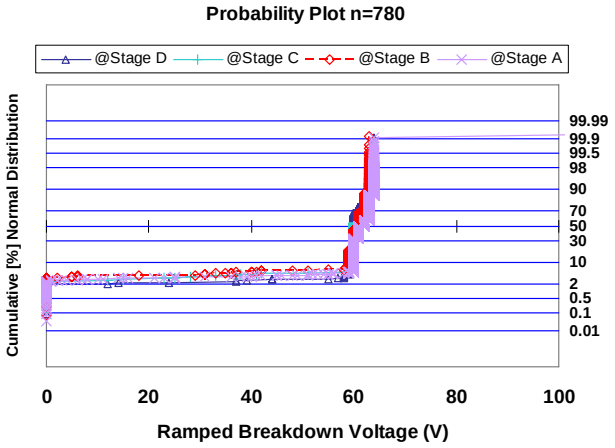

Figure 5 MIMCAP-On_Via Breakdown Probability Plots At 4 Test Stages. Test Vehicle is a capacitor with area 1,057,000um2

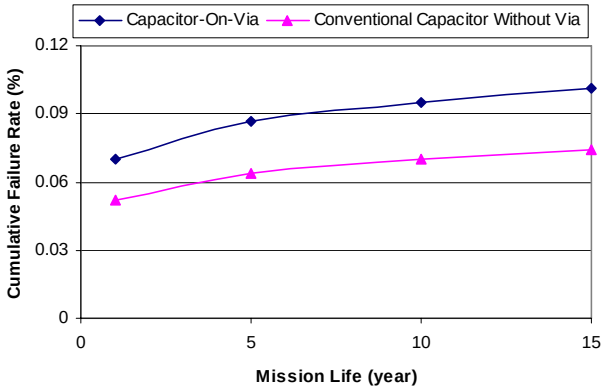

Figure 6 Reliability Prediction For Both MIMCAP-On-Via And Conventional MIMCAP Without Via After Thermal Cycles