

# Lifetime of SiN Capacitors Determined from Ramped Voltage and Constant Voltage Testing

H. C. Cramer, J. D. Oliver, and R. J. Porter

Northrop Grumman, Electronic Systems  
PO Box 1521 M/S 3K13, Baltimore MD 21203  
harlan.cramer@ngc.com Phone 410-765-0110

**Keywords: capacitor, dielectric breakdown, lifetime, ramped voltage, constant voltage, Linear Field Model, Reciprocal Field Model**

## ABSTRACT

**Understanding SiN capacitor dielectric integrity and reliability is becoming increasingly more important. For wide-bandgap semiconductor MMIC circuits bias voltages continue to increase: up to 40 or 50 volts for GaN HFET or MMIC devices and up to 100 V for SiC. Prior work on SiN dielectrics [1,2] emphasized applications for GaAs pHEMT and HBT devices where the applied voltages are around 5-15V. This paper reports on a study comparing the analysis methods and reliability determined from ramped voltage and constant voltage capacitor testing using both the Linear Field and Reciprocal Field Models in an attempt to characterize capacitor dielectrics.**

## INTRODUCTION

Failure of the SiN capacitors is second only to failure of the FET in limiting the life of compound semiconductor MMIC's. FET failure is easily noticed through a performance decrease and/or sometimes dramatic visual indications for "burned gates" or "craters". Capacitor failure is much more subtle. Visual indications are easily overlooked and performance changes resulting from cap shorts or opens may be incorrectly categorized as a change in FET parameters. In the extreme case, a failed capacitor may induce a FET failure and thereby be incorrectly attributed to the FET as the root cause.

The characteristic of the time dependent dielectric breakdown (TDDB) [3] model is that there is no single "breakdown voltage" but that the breakdown of the dielectric is a wear out mode, dependent upon the prior current and electric field applied to the device. This is consistent with the charge to breakdown model, which suggests that the dielectric will conduct a specific total charge before failure. The model has been further refined to suggest that the

total charge (current) that passes through the dielectric prior to breakdown may be dependent upon the particular conduction mechanism: ohmic for low voltage (linear in electric field) and Frenkel-Poole for high voltage (exponential in electric field) [3]. Lifetime testing requires accounting for the previously applied bias conditions.

Acceleration of dielectric failure occurs through both increases in electric field and temperature. In contrast to FET reliability studies, temperature acceleration is the less significant effect in dielectrics. Therefore, in reliability and lifetime studies, electric field is used to accelerate capacitor failures.

The literature reports two test methods for capacitor failure acceleration: ramped voltage, and constant voltage stress testing [2,5]. Also, two different models for lifetime prediction consider the (log of) lifetime to have either a linear or a reciprocal relationship to electric field. The controversy of whether to use a linear field model where lifetime is proportional to  $\sim \exp[-\gamma E]$  or a reciprocal field model where lifetime  $\sim \exp[G/E]$  is still not resolved. Suehle [4] suggests that the model may depend upon the fabrication method. In this study, the results of ramped voltage and constant voltage stress testing and comparisons of the estimated lifetime using both models are determined.

## FIELD DEPENDENT MODELS

For constant voltage testing the linear field model is given by:

$$t \propto \exp[-\gamma(E)]$$

Or using the reciprocal field model

$$t \propto \exp[G/(E)]$$

where:

t is the time to fail

$\gamma$  is the linear field acceleration factor

G is the reciprocal field acceleration factor

E is the electric field at the failure voltage

The ramped voltage failures can be transformed into constant voltage time predictions using a linear field model:

$$t = t(o) * \exp[\gamma(E_R - E)]$$

Or for the reciprocal field model:

$$t = [\exp(G/E)] * \Delta\tau * \sum_{i=1}^n \exp[-G/(\Delta E * i)]$$

where:

t(o) is the effective time constant given by:

$$t(o) = \frac{\Delta\tau}{1 - e^{-\gamma\Delta E}}$$

and where:

$\Delta\tau$  is the ramp step time

$\Delta E$  is the ramp step field

t is the time to failure at the operating voltage

$E_R$  is the field at the ramped voltage failure

E is the field at the operating voltage

i is the step counter

n is the failure step

$\Delta E * n$  is  $E_R$ , the field at the ramped voltage failure

The reciprocal field model for a ramped voltage transformation does not have a closed form representation. Numeric summation using finite voltage steps was used for the analysis.

#### TEST PROCEDURE

A dedicated process evaluation mask set which included numerous capacitors of various sizes, shapes and aspect ratios was utilized in this work [1]. The smallest size (12um x 12um) capacitors were tested to limit the potential for defects as much as possible. These capacitors are sufficiently small to be considered "intrinsic", and testing did not reveal early failure which is attributed to defects present in the nitride. Identical capacitors on the same wafers were used for both ramped and constant voltage testing.

Both ramped and constant voltage capacitor testing were conducted on-wafer utilizing a Keithley S900

parametric test system. Testing followed JESD35-A [6] with only a few differences. Failure was determined from evaluating current compliance, and for the constant voltage testing, changes in the capacitor value.

A nitride thickness of 160 nm was selected for convenience in testing. The failure voltage of thicker nitrides, (200-250 nm) exceeded the 200V maximum voltage of the parametric test system. Use of the 160 nm nitride allowed capture of the failure voltage of nearly all capacitors tested, but it was sufficiently thick to eliminate significant variability in the results from surface defects and roughness.

Constant bias voltage tests were conducted over the range 144V -178V and gave more than a three order of magnitude variation in test time (1 second to >4 hours per cap) and reported lifetime. Failure was determined by exceeding the current compliance of 10  $\mu$ A. In addition, to further evaluate the capacitors, the value of the capacitance was measured both prior to testing and post failure for the constant voltage tests. The sample size of 24 capacitors allowed the lower voltage testing to be completed in overnight and weekend blocks of time when the instrument was not required for regular production testing.

Ramped voltage testing consisted of 0.04 through 4V/sec ramp rates which were applied as a staircase, in steps of 0.2V, with step time varied to achieve the required ramp rate. Again, failure was determined by exceeding the current compliance of 10  $\mu$ A. Sample size was 48 or 96 capacitors, again a number which allowed convenient test times.

#### CONSTANT VOLTAGE RESULTS

The distribution of capacitor failures for constant voltage bias testing is shown in figure 1. The linearity and lack of early failures in the data indicates that the capacitors are nearly intrinsic or defect free. To extract the capacitor lifetime, the median failure time (t50) for each voltage was determined from curve fitting each of the individual curves. Then, in figure 2, the median lifetime is plotted with electric field and with the reciprocal of the field. Using a linear least squares regression, the slope determines the respective field acceleration factors. For the linear field model  $\gamma=40.2$  nm/V and, for the reciprocal field model  $G=40.3$  V/nm. Using these field acceleration factors, the predicted median lifetime at 50V bias is about  $10^6$  years for the linear field model, and approaches infinity ( $10^{30}$  years) for the reciprocal field model.

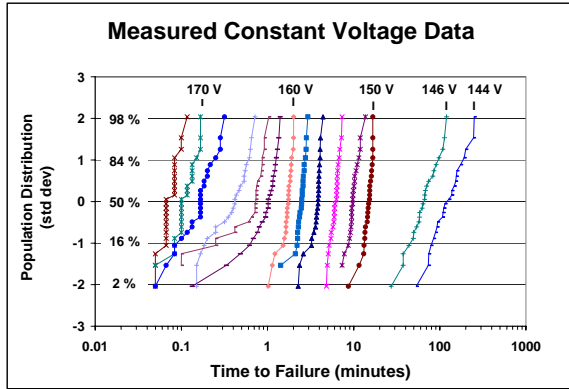


Figure 1. Constant voltage life test data for 12x12μm capacitors tested at 144 -172 volts.

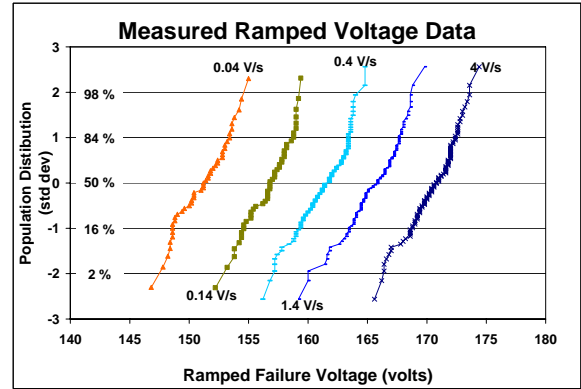


Figure 3. Measured ramped voltage life test data for capacitors tested at ramp rates of: 0.04, through 4.0 V/sec.

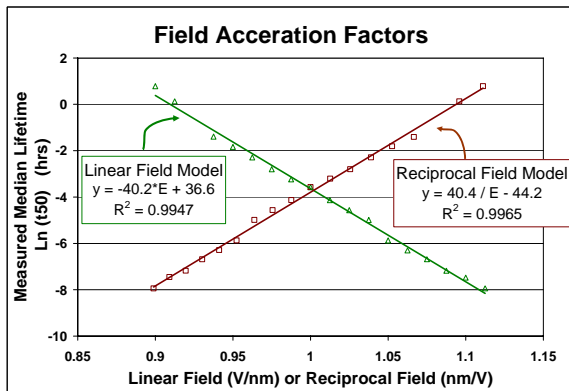


Figure 2. The median (50th percentile) lifetime is plotted to determine the field acceleration factor  $\gamma$  or  $G$  for the linear and reciprocal field models,

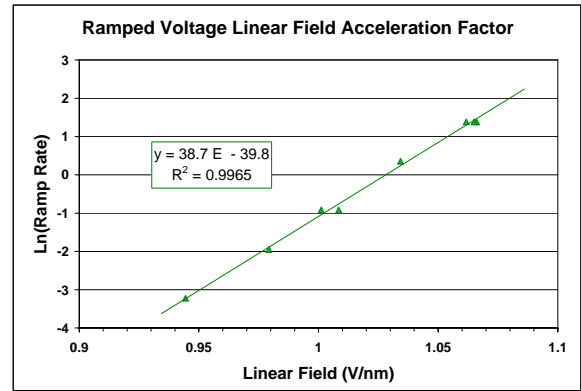


Figure 4. Field acceleration factor is determined from the slope of  $\ln(\text{ramp rate})$  vs. field for ramped voltage data.

## RAMPED VOLTAGE RESULTS

The distribution of failures for ramped voltage testing is shown in figure 3. Using the linear field model, the acceleration factor is determined from figure 4 where the ramp rate is plotted against the median electric field for each capacitor failure. The slope of a linear regression determines the field acceleration factor  $\gamma = 38.7 \text{ nm/V}$ . Using the reciprocal field model, numerically summing the contributions, and iterating for a least squares fit gives  $G = 35.5 \text{ V/nm}$ .

## DISCUSSION

Use of the linear field model for either ramped or constant voltage testing results in an equivalent field acceleration factor  $\gamma \sim 39 \text{ nm/V}$ . This value is self consistent and agrees reasonably with our prior work [1] where we reported  $\gamma \sim 36$  on a slightly different nitride process and with Yeats [2] who reported a

range on different wafers of  $\gamma \sim 35\text{--}43 \text{ nm/V}$  with a process average of  $38 \text{ nm/V}$ .

Use of the reciprocal field model resulted in a small difference between the calculated acceleration factor for constant voltage data,  $G \sim 40 \text{ V/nm}$  and for ramped voltage data,  $G \sim 36 \text{ V/nm}$ . Given that both values of the reciprocal field acceleration factor predict lifetime approaching infinity, the slight difference does not seem significant.

Lifetime predictions using the linear field model for both constant and ramped voltage data are shown in figure 5. The estimated lifetime difference between constant and ramped voltage data is less than an order of magnitude for both models (at 50 volts and 160 nm dielectric thickness). It is interesting to note that the acceleration factor derived from ramped voltage data is slightly less than the acceleration factor derived from constant voltage data. Yeats has also reported that ramped voltage testing underestimates

the lifetime when compared to constant voltage testing.

Based on this study we suggest adoption of the linear field model for intrinsic dielectrics. It is the more conservative model for the thicker nitride layers used for capacitors in MMIC processing. The silicon industry seems to prefer the reciprocal field model which appears to be more representative for the thinner dielectrics (higher fields and trap conduction mechanisms) used in Si MOS processing.

Realistic capacitors, (extrinsic capacitors, e.g. those with defects in dielectric or metal plates) may have significantly shorter lifetimes. This is evidenced by the increased number of capacitors failing at lower than the predicted voltage, i.e. "early failures". From a product standpoint, the intrinsic dielectric lifetime is so long that, except for high voltages (>80V), defects causing early failures are the only critical issues. Future work should concentrate on evaluating the methods to best understand and analyze the failures caused by defects.

Constant voltage testing at high voltages may be designed to have shorter test times than ramped testing, and thus could be suited for study of the intrinsic nitride failure. However, since the ultimate lifetime of the capacitor is unknown prior to testing; the actual length of the testing is indeterminate until the test is complete. Ramped voltage testing has a defined endpoint, the maximum system voltage. For general testing then, a ramped voltage test is preferred since it is relatively fast and, as a result of the step increased voltage, capacitor failure (or at least test completion) is assured in a time determined by the ramp rate. Also ramped voltage testing allows for better resolution of the early failures and so is

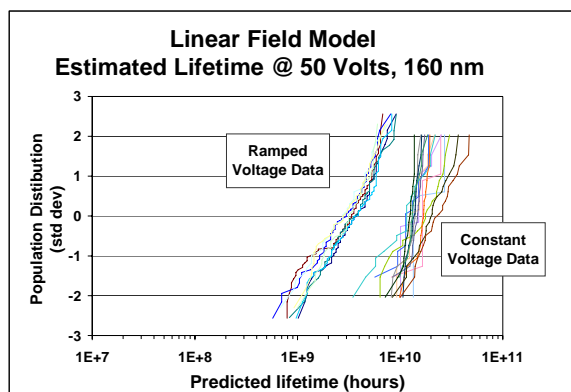


Figure 5. Estimated lifetime for a bias of 50V predicted from both ramped and constant voltage data using the linear field model.

suited to the more important study of defect effects in nitride lifetime. As this work has shown, the intrinsic lifetime of silicon nitride dielectrics is sufficiently long and essentially inconsequential in determining device reliability. The only reliability limiting effects are the early failures. Ramped voltage testing is well suited to identify these effects.

#### SUMMARY

The failure of SiN dielectrics was characterized using both ramped voltage and constant voltage capacitor test methods. Testing of intrinsic capacitors (small, no defects) was used to determine the electric field acceleration factors and predict lifetime using both the Linear and Reciprocal Field Models. The linear field acceleration factors determined from ramped voltage and constant voltage testing are identical ( $\gamma \sim 39$  nm/V) showing that either method may be used for the evaluation of dielectric reliability. This study suggests adoption of the linear field model. It produces more realistic and more conservative lifetime predictions. Practical considerations related to test time and equipment suggest ramped voltage testing allows more careful study of early failures or defects which are the reliability limiting factor.

#### REFERENCES:

1. H. Cramer, J. Oliver, G. Dix, M. Zimmerman, "Development of an Improved Capacitor Dielectric" Digest of 1998 International Conf. GaAs Manufacturing Technology Seattle WA p.15 1998
2. B. Yeats, "Assessing the Reliability of Silicon Nitride Capacitors in a GaAs IC Process," IEEE Transactions on Electron Devices, Vol. 45, No. 4, April 1998, p. 939.
3. J. Scarpulla, D. Eng, S. Olson, C Wu, "A TDDB Model of Si<sub>3</sub>N<sub>4</sub> - Based Capacitors in GaAs MMICs" Proceedings IEEE 37th International Reliability Physics Symposium, San Diego CA p.128 1999
4. J. Suehle, P. Chaparala, C. Messick, W. Miller, K. Boyko, "Field and Temperature Acceleration of Time-Dependent Dielectric Breakdown in Intrinsic Thin SiO<sub>2</sub>, 1994 International Reliability Physics Symposium p.120 1994
5. A. Berman, "Time-Zero Dielectric Reliability Test by a Ramp Method," in 1981 Int. Reliability Phys. Symposium, 1981, p. 204.
6. "Procedure for the Wafer-Level Testing of Thin Dielectrics", JEDEC Solid State Technology Association 2500 Wilson Boulevard Arlington, Virginia 22201-3834

#### ACRONYMS

t<sub>50</sub>: median failure time