# A 3.3 fF/μm$^2$ 40 V BST MIM capacitor suitable for above MMIC integration

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## Abstract

**A high performance metal-insulator-metal (MIM) capacitor with $Ba_{(1-x)}Sr_xTiO_3$ (BST) films deposited at 200°C is presented for the first time. Through a detailed analysis of the relationship between BST crystallographic structures and its electrical characteristics, a triple-layered BST structure was found to be effective in suppressing leakage current and hence increasing breakdown voltage while maintaining a high capacitance density. By using the triple-layered BST structure, an excellent MIM capacitor with a capacitance density of 3.3 fF/μm$^2$, a breakdown voltage of 40 V and an insertion loss below 0.05 dB has been successfully obtained. This MIM capacitor can be easily integrated into conventional microwave monolithic integrated circuits (MMICs).**

## INTRODUCTION

An essential component for high performance mobile handsets is a MIM capacitor that has a large capacitance density, a high breakdown voltage, and good RF characteristics, such as low insertion loss. A MIM capacitor with a SiN film as a dielectric material is usually used due to its easy fabrication. However, as the capacitance density of the SiN MIM capacitor is relatively low (0.4 - 1 fF/μm$^2$) [1], other high-k films are better suited for fabrication. Some polycrystalline films with a perovskite structure such as $SrTiO_3$ (STO), $BaTiO_3$ (BTO), BST and $PbZn_{(1-x)}Ti_xO_3$ (PZT) are well known as high-k materials. Among these, the BST film has a high dielectric constant and a low dielectric hysteresis, which results in low harmonic distortion (HD) and low intermodulation distortion (IMD). We believe that the BST film is the best candidate for use as a dielectric material of a MIM capacitor that is used in high frequency applications.

A conventional BST film is deposited at temperatures greater than 500°C to obtain a high dielectric constant caused by good crystallinity and large grain size [2]. However, for a MIM capacitor with a BST film, the high temperature process often gives rise to large leakage currents, resulting in a lowering of the breakdown voltage. As a result, this substantially restricts the application field for the BST films. For instance, this film cannot be integrated into the backend processes of MMICs because the resistance of the metal ohmic contact significantly increases when thermal treatment exceeds 350°C. Therefore, it is necessary to develop a BST formation technique that enables materials when a high dielectric constant and a low leakage current (or high breakdown voltage) to be produced at low temperatures. However, there have been few reports focusing on the electrical characteristics of BST films deposited at low temperatures.

In this paper, a two-step BST deposition technique is proposed for the first time that meets the above-mentioned strict requirements. A triple-layered BST structure was formed using the proposed technique. Furthermore, a MIM capacitor with a BST film showed excellent electrical characteristics despite being fabricated at a low temperature.

## EXPERIMENTS

Figure 1 shows the main steps in fabricating a MIM capacitor. After a 300-nm-thick SiN film was formed by plasma enhanced chemical vapor deposition (PECVD) on a GaAs wafer, 50-nm-thick Ti and 200-nm-thick Pt were sequentially deposited by a DC sputtering method to create a bottom electrode. Following this, the 100-nm-thick BST film was deposited by an RF magnetron sputtering method. Here, as shown in Fig. 1, two deposition processes (i.e. one- and two-step deposition) were used to create a multi-layered structure in the BST film. For the one-step deposition process, deposition temperatures of 100, 200, and 300°C were used so that the MIM capacitor could be easily fabricated at the backend process of MMICs with a sufficient temperature margin. On the other hand, for the two-step depositionprocess, only 200°C temperature was selected, and a 70-nm-thick BST film was deposited in the first step. Process conditions, except for the temperature, were the same as those for the one-step deposition process. After the first step, all process gasses were exhausted to the base pressure and then, as the second step, a 30-nm-thick BST film was deposited. The BST film was then patterned and the bottom electrode was formed. Finally, 100-nm-thick Pt and 400-nm-thick Au films were sequentially deposited by a DC sputtering method and an evaporation method, and then patterned as a top electrode. This completed the MIM capacitor fabrication.

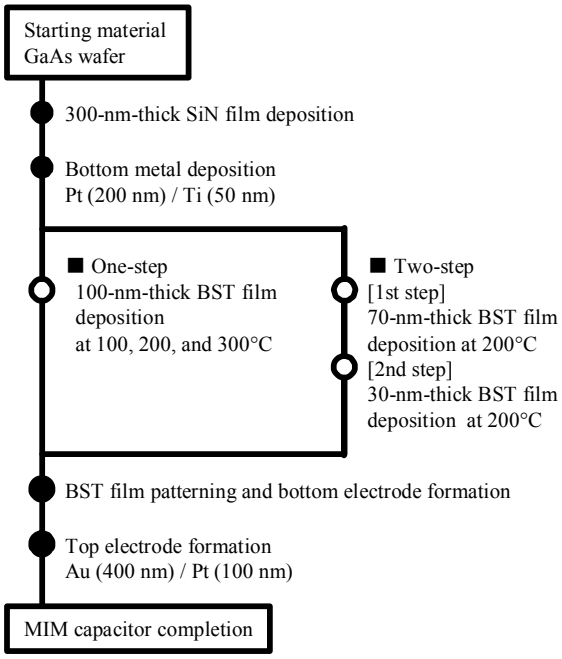


Fig. 1 Main step in fabricating MIMC.

The measurement systems used here are as follows. The capacitances were measured using a LCR meter. The leakage currents were measured using a parameter analyzer. The insertion losses were measured using a network analyzer. The HDs and the IMDs were measured using a spectral analyzer. The measured MIM capacitors' size was 100 µm x 100 µm.

The crystallographic characteristics of the BST films were evaluated by TEM and electron beam diffraction.

## RESULTS AND DISCUSSION

Figure 2 shows the leakage current characteristics of MIM capacitor fabricated by the one-step deposition process. The BST films were deposited at 100 and 200°C. The applied voltage indicates the bias at the top electrode. The leakage current depends on the bias direction, and therefore the I-V characteristics were asymmetric. In the negative bias region of less than – 10 V, the leakage currents of the 100-°C-deposited BST film were clearly lower than those of the 200-°C-deposited BST film. Fig. 3 shows the capacitance density and the breakdown voltage dependence on deposition temperature. Here, we defined the breakdown voltage as the voltage in the negative bias region when the leakage current reached 2 nA/pF. By lowering the deposition temperature, the breakdown voltage increased, whereas the capacitance density decreased. Therefore, lowering the deposition temperature is ineffective in increasing the breakdown voltage while maintaining a high capacitance density.

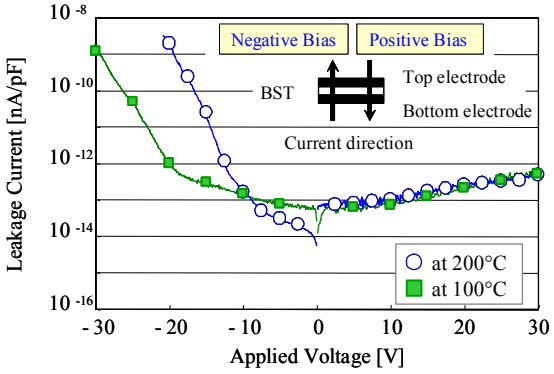


Fig. 2 I-V characteristics of BST film fabricated by one-step deposition process.

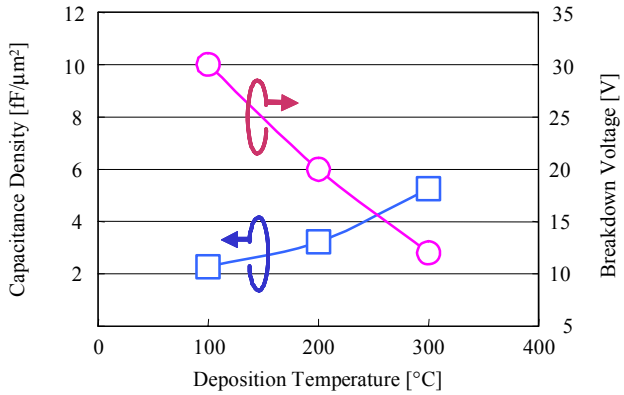


Fig. 3 Capacitance and breakdown voltage as a function of BST deposition temperature for one-step deposition process.

Figure 4 shows the leakage current characteristics for the two-step deposition process at 200°C. For comparative purposes, the leakage current characteristics for the one-step deposition process are also drawn. The two-step deposition clearly reduced the leakage current.

Figure 5(a) shows a cross-sectional TEM image of the BST film formed by the one-step deposition process at 200°C. In this photograph, the BST film is composed of two layers; the first layer is amorphous, and the second layer is polycrystalline with a columnar structure.

In general, a lattice-matching between the BST film and the bottom electrode also affects the crystal growth of BST as well as the deposition temperature. Therefore Pt, Ru, and SoRuO3(SRO) were used as the bottom electrode because their lattice constants are close to that of BST. However, even with similar lattice constants, the crystallinity of the initial part of the BST film was not good, and the crystallinity of the later part of the BST film achieved a high quality. These characteristics of BST crystalline growth were even more significant at low temperature deposition. We believe that the asymmetric I-V

characteristics shown in Fig. 2 are caused by this double-layered structure.

Figure 5(b) shows a cross-sectional TEM image of the BST film formed by the two-step deposition process at 200°C. The BST film fabricated in the first-step was composed of two layers as shown. Afterwards, the BST film fabricated in the second-step composed a third layer that was polycrystalline. In the TEM image shown in Fig. 5(b), there seems to be a boundary between the second layer of the first-step deposition and the third layer fabricated at the second-step deposition, and both layers are polycrystalline. So, the two-step deposition process produces a triple-layered structure in the BST films.

The BST film with this triple-layered structure was analyzed by an electron diffraction method and a dark field TEM. Results are shown in Fig. 6. Photographs A and B show the diffraction patterns for the third and second layers, respectively. These patterns indicate a columnar polycrystalline structure with different crystal orientations. This difference in crystal orientation causes a difference in contrast between the dark field TEM image of the second and third layers. This triple-layered structure in the BST film had a horizontal boundary between the second and third layers with different crystal orientations. The results shown in Fig. 4 imply that any boundary layer, such as a thin amorphous layer that exists between the second and third layers, may play a crucial role in reducing leakage currents in the negative bias region.

Figure 7 shows the capacitance and breakdown voltage of the BST films fabricated by the one-step and two-step deposition processes. This figure also shows the usefulness of the triple-layered structure fabricated by the two-step deposition process. A breakdown voltage of 40 V was achieved while maintaining a high capacitance density of 3.3 fF/μm$^2$. This capacitance density was achieved because the third layer was polycrystalline and not amorphous. This 40-V breakdown voltage is very important for next generation MMICs for mobile handsets. The output

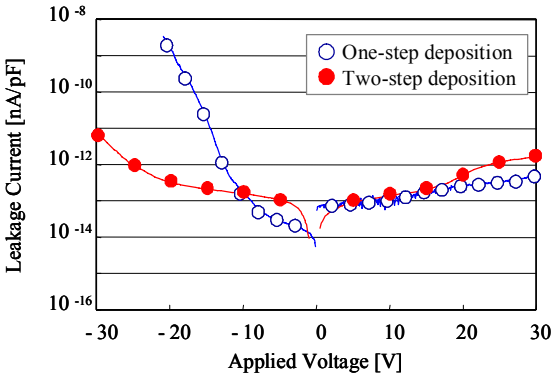


Fig. 4 I-V characteristics of BST film deposited by one-step and two-step deposition processes.

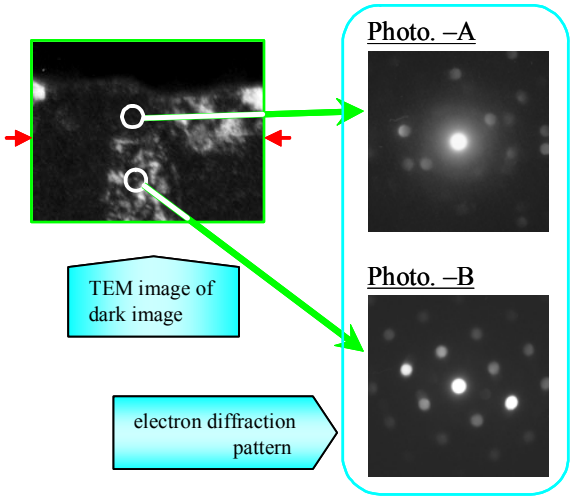


Fig. 6 Cross sectional TEM image of dark image and electron diffraction pattern of BST film. Third-layer (Photo-A) and second-layer (Photo-B) .

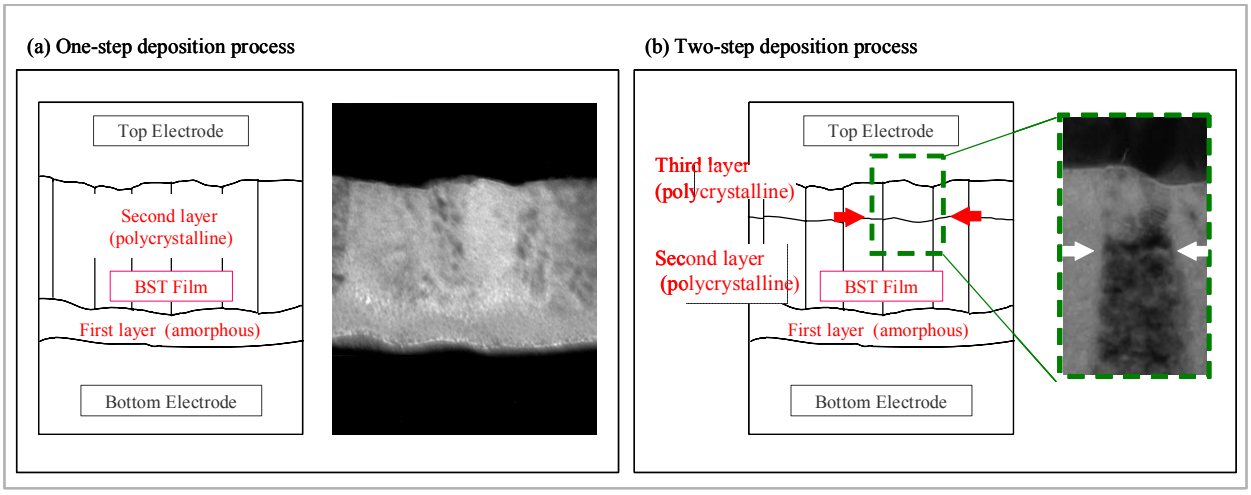


Fig. 5 Cross-sectional TEM images of BST films. (a) one-step deposition process and (b) two-step deposition process.

power for mobile handsets will be 34 dBm, which when converted is equal to about 20 V maximum-applied voltage to the BST MIM capacitor. So, the breakdown voltage of MIM capacitor should be greater than 30 V with a margin. This MIM capacitor can be effectively applied for any DC-blocking device, such as a decoupling condenser.

We also evaluated the high-frequency characteristics of the BST MIM capacitor. Table 1 lists the characteristics of the BST MIM capacitor formed by the two-step deposition method. The capacitance was independent to the frequency up to 5 GHz. The insertion loss was less than 0.05 dB from 0.7 GHz to 7 GHz, as shown in Fig. 8. The HD and the IMD were suppressed below -55 dBm and -120 dBm.

The low insertion loss in this frequency region is useful for next generation of MMICs for mobile handsets. These good RF characteristics would enable the present MIM capacitor to be integrated in a RF signal line with low signal loss and low signal distortion.

## CONCLUSIONS

We developed a new two-step deposition method that achieved a breakdown voltage of 40 V while maintaining a high capacitance density of 3.3 fF/μm$^2$ in low temperature process of 200°C. This method makes it possible to fabricate a high performance MIM capacitor above a MMIC for mobile handsets.

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## ACRONYMS

MIM: Metal Insulator Metal
MMIC: microwave monolithic integrated circuit
BST: $Ba_{(1-x)}Sr_xTiO_3$
STO: $SrTiO_3$
BTO: $BaTiO_3$
PZT: $Pb_{(1-x)}Zn_xTiO_3$
HD: Harmonic Distortion
IMD: intermodulation distortion
PECVD: Plasma Enhanced Chemical Vapor Deposition
TEM: Transmission Electron Microscopy

Table 1
BST MIMC performance

| Items | | Characteristics |
|---|---|---|
| Capacitance density | 0.1-5.0 GHz | 3.3 fF/μm$^2$ |
| Breakdown Voltage | 2 nA/pF | 40 V |
| Insertion Loss | 0.7-7.0 GHz | < 0.05dB |
| Harmonic Distortion | 2nd & 3rd | − 55 dBm |
| IMD | 2nd & 3rd | -120 dBm |

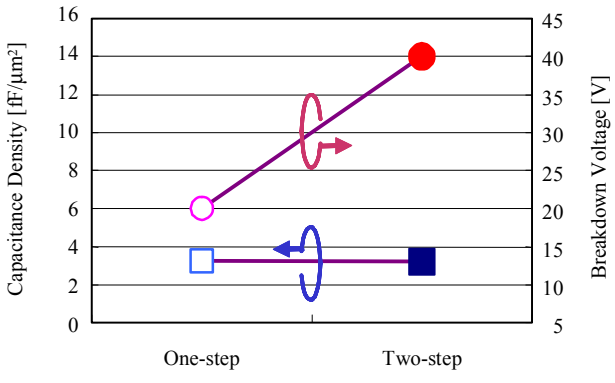


Fig. 7 Capacitance and breakdown voltage of BST film fabricated by two deposition processes (at 200°C).

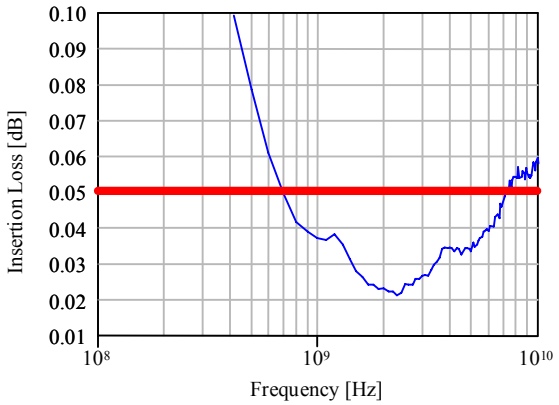


Fig.8 Insertion loss as a function of frequency.