Status and Progress in InP Optoelectronic Processing: Towards Higher Levels of Integration

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Keywords: InP, optoelectronic devices, monolithic integration, yield management, process control, manufacturing

Abstract

The status and progress of InP optoelectronic integration is reviewed. It is shown that Infinera has been able to commercialize large-scale photonic integrated circuits with more than 50 components on a single InP chip through a set of well controlled processes and robust component designs. The architecture and performance of Infinera's PICs is described, along with relevant yield and production metrics that make this platform at once manufacturable and scalable.

INTRODUCTION

Since the early demonstrations of InP optoelectronic components it was believed that the integration density of these devices would increase over time, similar to the progress made by the Silicon IC industry. However, the progress in photonic integration density has not been as rapid as expected. Several research demonstrations of multi-component devices have been shown, but commercial realization has been limited. In the late nineties, multi-component devices such as EMLs were introduced, which consist of a DFB laser and an electro-absorption modulator. Several years later, devices with more components were commercialized, but had typically no more than 4 components per device. In 2004 Infinera announced that they had achieved live-traffic in the field over their network systems, which contain photonic integrated circuits with more than 50 components integrated on a single InP chip. This demonstrates that large-scale photonic integrated circuits can be manufactured with sufficient yield, performance, and reliability to meet all requirements for economically viable production.

INP PHOTONIC INTEGRATED CIRCUITS

The initial slow progress in integration density for InP optoelectronic devices is shown in Fig. 1, where the number of components is shown for InP transmitter devices utilized in telecommunication networks. In the first 20 years, from 1980 to 2000, the commercially available devices consisted of only 1 and later 2 components. By 2003, new devices, such as tunable EMLs with integrated SOAs, were introduced which consisted of a few components. However, it was not until 2004 that the first large scale photonic integrated transmitter chips were commercialized by Infinera. Their LS-PICs are used in their Digital Optical Networking Systems, where each PIC handles 100 Gbit/s of data [1]. The transmit PIC consists of an AWG multiplexer and 10 transmit channels which each consist of a tunable DFB laser, a 10 Gbit/s EAM, a VOA, and a power monitor photodiode, all integrated on a single InP transmit (Tx)PIC chip (cf. Fig. 2a). The receive PIC consists of an AWG demultiplexer and 10 receive channels which each have a high-speed photodiode, all integrated on a single InP receive (Rx)PIC chip (cf. Fig. 2b).

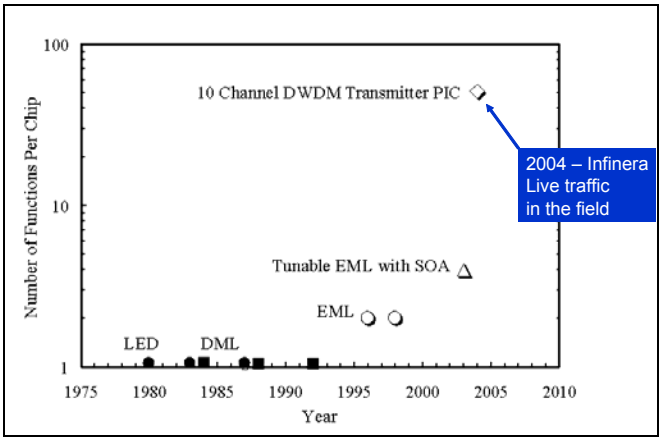

Figure 1. Growth of the number of integrated components in InP based transmitter chips used in telecommunication networks.

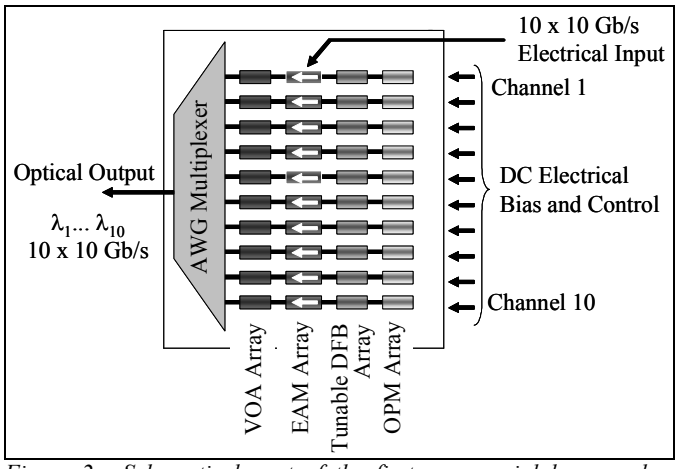

Figure 2a. Schematic layout of the first commercial large-scale photonic integrated circuit, a DWDM transmit PIC.

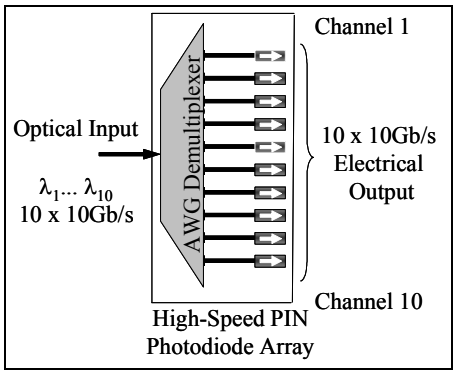

Figure 2b. Schematic layout of a DWDM receive PIC.

YIELD MANAGEMENT

By increasing the amount of components integrated on a single chip, the die-size also increases. This typically entails a reduction in chip yield and it was generally expected that the integration of many optoelectronic components onto a single InP chip would not be economically feasible. However, Infinera has been able to manufacture LS-PICs with acceptable yields for cost-effective commercialization. This was achieved by a set of well controlled manufacturing processes and robust component designs.

From yield calculations performed on data from our testers, using a negative binomial distribution, we can extract the random yield, systematic yield, fatal defect density, and cluster factor [2, 3]. In Fig. 3, the random yield curve is shown for the manufacturing process of a TxPIC, as well as a comparison with random yield curves of the Si IC industry from 3 different years. The Infinera InP curve corresponds roughly with the Si IC industry curve of 1987.

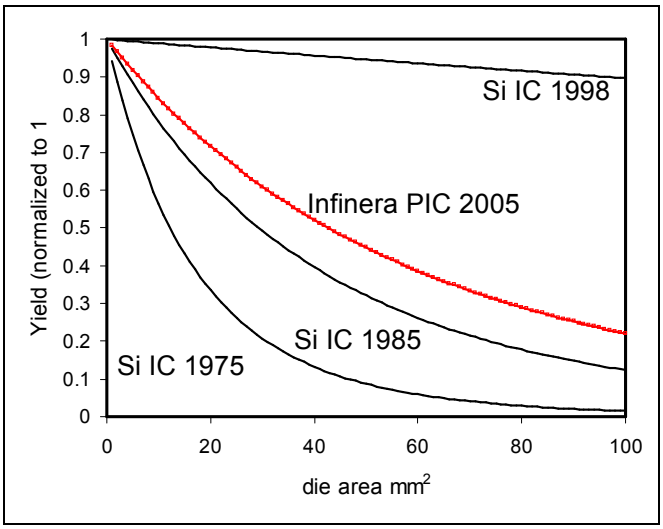

Figure 3. Yield curve for Infinera's TxPIC, together with yield curves of the Si IC industry for 1975, 1985, and 1998.

It must be noted that, compared to the Si IC industry, the InP manufacturing processes are not as mature and advanced. For InP, the wafer size is much smaller, the tool set is less sophisticated, and the processes are less standardized. As a result, more manual wafer handling takes place and the particle density is higher. However, for InP photonic integrated circuits, the waveguides are a few um wide, and the optical wavelength in the material is around 0.5um. Therefore, the typical killer defect size is much larger than in the modern Si IC industry. For InP, defects of 1um or less are usually harmless for performance and reliability. Only defects of several microns or larger cause yield loss. Therefore, even with less advanced manufacturing processes, the chip yield of InP photonic devices can be high. Clearly, over time, as the processes mature, there is no reason to believe that the yield will not continue to rise. This will allow larger die-size with acceptable yield and hence a further scaling of integration density.

At Infinera, we have established an advanced process control system. Statistical process control (SPC) is practiced for all manufacturing tools and processes (cf. Figs. 4 and 5). We also use real-time product SPC, together with documented and proven out-of-control action plans (OCAPs), to keep all processes in control. This is done throughout the manufacturing area, including epi, wafer fab, die fab, assembly, burn-in, and test. Special monitor lots and in-line test structures on product wafers provide rapid feedback into the tool settings in a closed-loop, continuously monitored system. Process capability data and parameter distributions are fed back to device engineers so that they can make design improvements and help to ensure that future designs will make optimum use of trade-offs among parameter values and yield. This process control system is vital to the management of our PIC manufacturing operations.

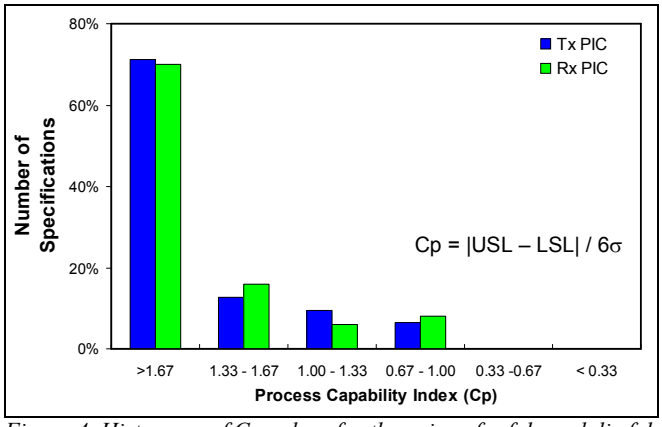

Figure 4. Histogram of Cp values for the epi, wafer fab, and die fab manufacturing processes for both the RxPIC and TxPIC devices. Note that ~95% of all processes have a Cp larger than 1.0.

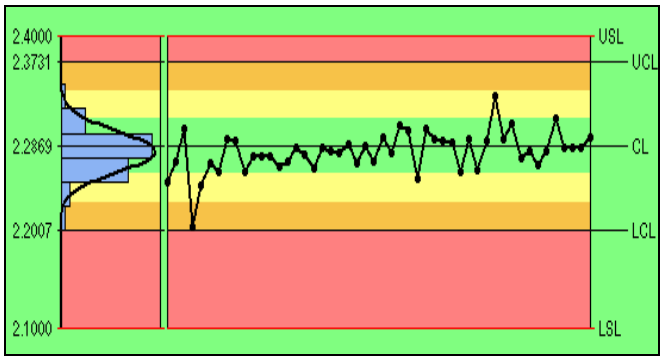

Figure 5. Example of an SPC chart, in this case for one of the etch depths of the TxPIC. Cpk for this process is 2.18.

PERFORMANCE OF THE LS-PIC

For optical chips we clearly also need to evaluate the optical performance, which is done after singulation and mounting of the devices onto carriers. This so-called CoC testing is done with RF probes on the modulator and with a fiber to the in/output waveguide. These tests will provide conditions very similar to actual deployment field data. We have access to 10 Gbit/s frequency modulation data, as well as the optical spectrum for crosstalk, linewidth, SMSR, etc.

For the TxPIC each of the 10 channels need to meet all specification limits, i.e. we need a comb of 10 accurate and stable DFB wavelengths centered on the ITU grid. Also the fiber output power and modulator RF performance need to be accurately measured and controlled to meet the required product specifications. This is one of the most challenging aspects of our PICs. With a set of well designed components, tightly controlled fabrication processes, and active feedback, we have achieved a high-yielding process. In Fig. 6 we show some graphs of the device performance distributions of the TxPIC, which indicate that the PIC yields to critical optical specifications are very high.

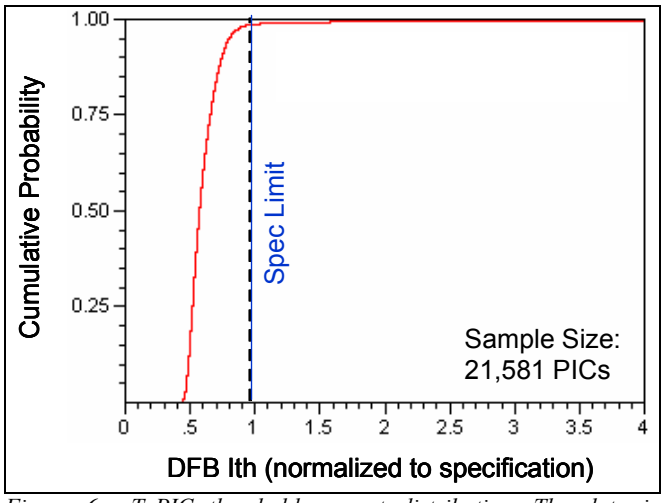

Figure 6a. TxPIC threshold current distribution. The data is normalized to the specification limit. This plot shows the threshold current of the worst channel of each PIC. This distribution comprises over 20,000 PICs.

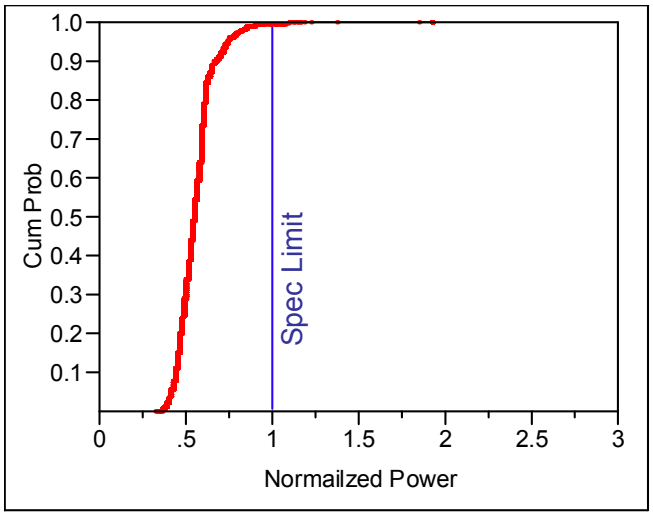

Figure 6b. TxPIC launched fiber power per channel at final CoC test (before module packaging). The data is normalized to the specification limit. This plot shows the power of the worst channel of each PIC. This distribution comprises all TxPICs measured in 2005.

The RxPIC has fewer components and is easier to characterize than the TxPIC. It also has far fewer specifications. Responsivity, dark current density, electrical bandwidth, polarization dependence, and crosstalk are some of the main parameters of interest for the RxPIC. Some examples of performance distributions of RxPIC are shown in Fig. 7. These distributions show that the manufacturing processes and designs employed to produce these devices are very capable of high yields.

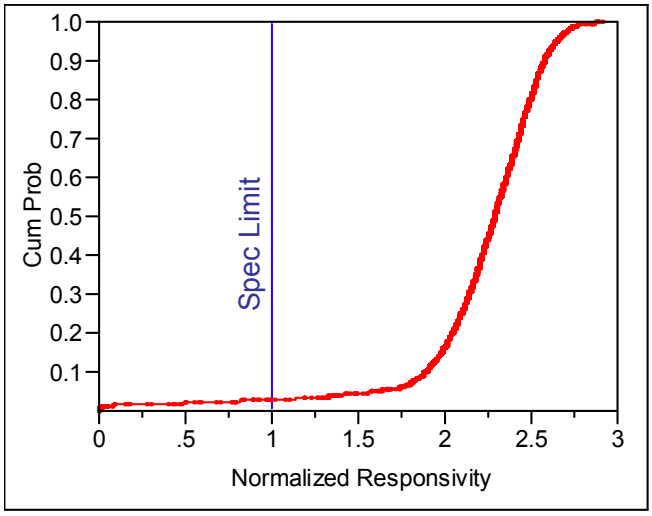

Figure 7a. CoC test data for responsivity of the RxPIC. The data is normalized to the specification limit. This plot shows the responsivity of the worst channel of each PIC. This distribution comprises all RxPICs measured in 2005.

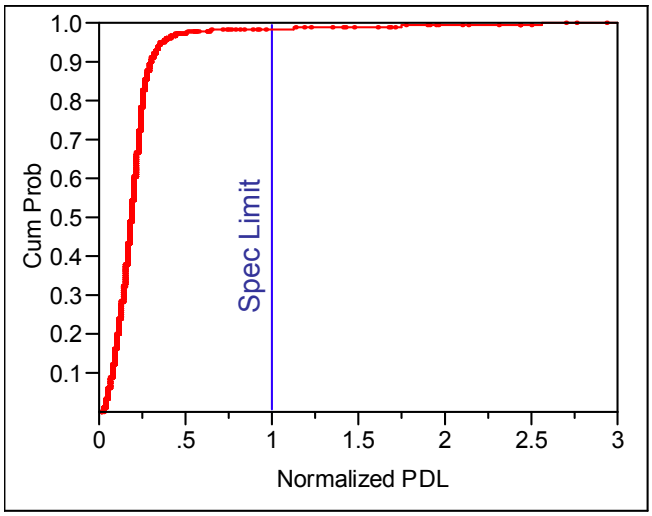

Figure 7b. CoC test data for polarization dependent loss of the RxPIC. The data is normalized to the specification limit. This plot shows the PDL of the worst channel of each PIC. This distribution comprises all RxPICs measured in 2005.

As shown above, the final CoC test performance yields are not an inhibitor to LS-PICs, when the component designs are robust and tolerant, and the manufacturing processes are actively controlled with an integrated yield management system.

RELIABILITY OF THE LS-PIC

In the sections above we only looked at so-called beginning-of-life PIC data. A very important aspect of all telecom devices is the reliability of the product over life. Typically, a component's life has to be guaranteed to be at least 20 years. We subject our PICs to accelerated aging under various conditions to learn about the product reliability and failure modes. Both RxPIC and TxPIC have undergone extensive reliability testing (>2.4 x 10^7 actual device hours) and have been qualified according to GR-468. In addition, the many control and sense elements in the PIC, module and system allow reliability data to be periodically collected during operation in the field. In the first year of deployment, we have collected over 1 million hours of PIC operating data without a single PIC failure. Fig. 8 shows the DFB power shift for all channels of a TxPIC module for a period of 8000 hours, obtained from a system carrying live traffic. Clearly, the output power is extremely stable over time.

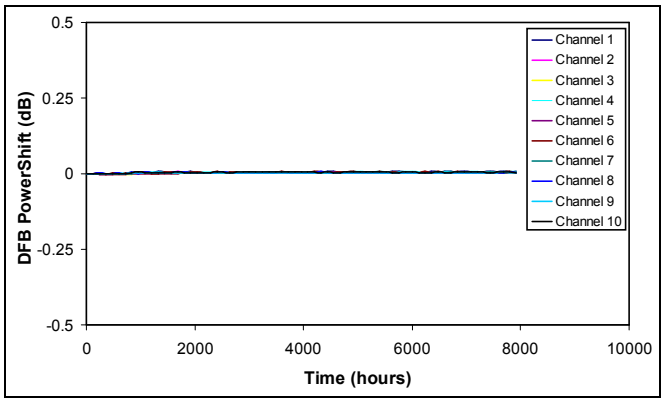

Figure 8. DFB optical power drift for all channels of a TxPIC under operation, obtained from a module carrying live-traffic in the field.

CONCLUSIONS

We have shown that it is possible to manufacture complex large-scale photonic integrated circuits with acceptable yield, device performance, and reliability, to allow cost-effective commercialization of such devices. Infinera has achieved this by means of robust and tolerant device designs, rigorous and tight process control, and an integrated yield management system.

ACKNOWLEDGEMENTS

The authors would like to thank all personnel at Infinera, for their contribution to this work.

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ACRONYMS

AWG: Arrayed Waveguide Grating
CoC: Chip on Carrier
EAM: Electro-Absorption Modulator
LS-PIC: Large Scale Photonic Integrated Circuit
PIC: Photonic Integrated Circuit
VOA: Variable Optical Attenuator