Compound Semiconductor MOSFET Structure With High-κ Dielectric

Karthik Rajagopalan, Ravi Drooopad, Jon Abrokwah, Matthias Passlack

Freescale Semiconductor, Inc., 2100, E Elliott Road, Tempe, AZ-85284.
karthik.rajagopalan@freescale.com 480-413-7032

Keywords: III-V MOSFET, high mobility MOSFET, GaAs MOSFET

Abstract

MOS heterostructures grown by molecular beam epitaxy on III-V substrates, employing a high-κ dielectric ($\kappa \approx 20$) have been fabricated. Mobilities exceeding 12,000 cm^2/Vs and 6,000 cm^2/Vs, for sheet carrier concentration $n_s \approx 2.5x10^{12}$ cm^{-2} were measured from MOSFET structures grown on InP and GaAs substrates respectively. These structures were designed for enhancement mode operation and include a 10nm thick strained $In_xGa_{1-x}As$ channel layer with In mole fraction x of 0.3 and 0.75 on GaAs and InP substrates, respectively.

INTRODUCTION

Advancements in the performance of CMOS devices employing silicon substrates have been consistently achieved by shrinking critical MOSFET dimensions. While critical dimensions keep decreasing to meet the demand for smaller and faster chips, the associated challenges will become increasingly difficult to address. High-κ dielectrics such as HfO_2 which are needed for smaller Si MOSFET's, reduce the electron mobilities from 500-600 cm^2/V-s to about 200 cm^2/V-s (for an inversion charge density of 2-3 $\times$ 10^{12} cm^{-2}) [1]. As theoretical limits are reached in the silicon CMOS world, references to MOSFETs based on compound semiconductor substrates have appeared in the International Technology Roadmap for Semiconductors [2] as possible candidates for future CMOS technologies. Presented here is a heterostructure with a high-κ dielectric, grown by molecular beam epitaxy (MBE) on a GaAs or an InP substrate. For a sheet carrier concentration of 2.5 $\times$ 10^{12} cm^2/V-s, electron mobilities in excess of 6,000 and 12,000 cm^2/V-s, respectively, have been measured.

STRUCTURE

The NMOSFET structure shown in Fig. 1 was grown on a 3 in. GaAs substrate by molecular beam epitaxy (MBE) using an Ultra-High Vacuum (UHV) dual chamber configuration tool manufactured by DCA. The GaAs epitaxial structure is grown in one chamber and then transferred through a UHV module to the second chamber where the gate oxide is grown. The epitaxial structure consists of a 0.2-μm undoped GaAs buffer layer, a 65nm undoped $Al_{0.3}Ga_{0.7}As$ layer, a bottom Si δ-doping, an undoped bottom spacer layer including 3 nm of $Al_{0.3}Ga_{0.7}As$ and 2nm of GaAs, a 10nm undoped $In_yGa_{1-y}As$ ($0.27 \leq y \leq 0.31$) channel layer, a 2nm undoped GaAs top spacer layer, a top Si δ-doping, a 2nm undoped $Al_{0.45}Ga_{0.55}As$ barrier layer and a 20nm amorphous $Ga_2O_3/(Gd_xGa_{1-x})_2O_3$ dielectric stack. This dielectric stack consists of a thin (10-12Å) template layer of Ga_2O_3 followed by a bulk ternary $(Gd_xGa_{1-x})_2O_3$ layer. The Ga_2O_3 layer provides for the unpinning of the GaAs Fermi level while the $(Gd_xGa_{1-x})_2O_3$ forms the bulk of the dielectric stack. More details of the growth process can be found in [3].

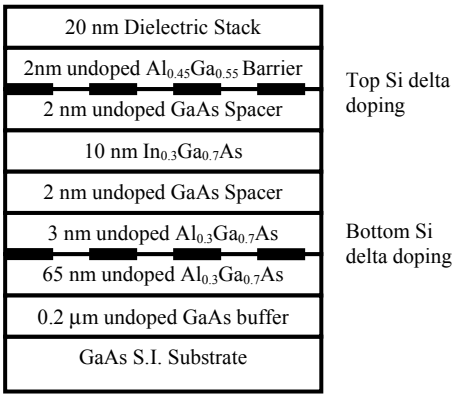

Fig. 1. NMOSFET structure on GaAs substrate

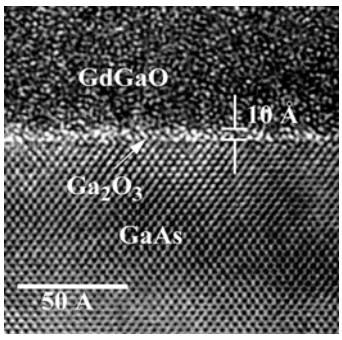

Fig. 2. TEM image of the gate dielectric stack

Typical electrical parameters of the dielectric stack, such as midgap interface state density of ≈2 × 10^{11} $cm^{-2}eV^{-1}$ on GaAs and a dielectric constant κ of 20, were reported in [4], [5].

Fig. 2 shows a TEM image of the gate oxide stack on GaAs. The Ga_2O_3 template layer and $(Gd_xGa_{1-x})_2O_3$ (x ≈ 0.6) layer can be seen clearly in the image. A similar structure was also grown, as mentioned above, on InP substrate, with 75% In in the channel. For reference purposes, a standard pseudomorphic high electron mobility transistor (PHEMT) structure in which the gate dielectric was replaced by a 30nm GaAs cap layer was also grown on GaAs.

RESULTS

NMOSFET electron transport properties have been obtained by a non-contact measurement method, using the Lehighton Electronics Model 1610 Nondestructive Mobility Measurement System. The non-contact transport data has been verified by Lehighton to be within 10% of standard DC Hall measurements and the difference between Hall mobilities and effective channel mobilities determined by the split C-V method is typically less than 10% [1], [6].

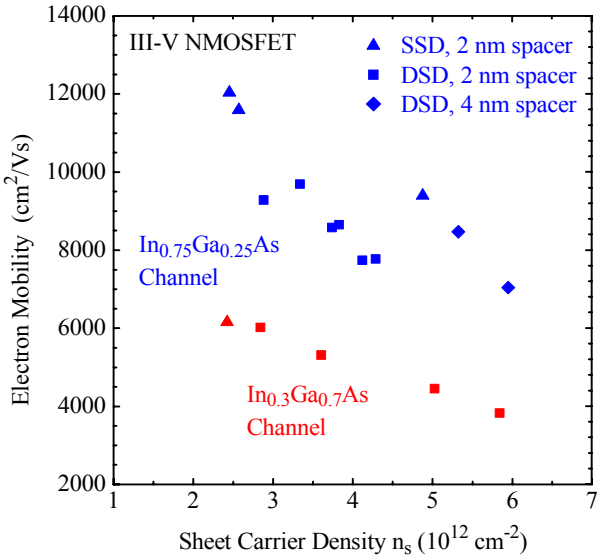

Fig. 3. Mobility vs Sheet carrier density

Fig. 3 shows the measured transport data for NMOSFET structures on GaAs and InP substrates, as a function of sheet carrier density (n_s) for various top δ-doping concentrations. For MOSFET structures on GaAs, the bottom δ-doping concentration was fixed at 6 × 10^{12} cm^{-2}. The top δ-doping concentration was varied from no top δ-doping to 6 × 10^{12} cm^{-2}. In Fig. 3 solid triangles represent Single Sided Doping (SSD) and solid squares/diamonds represent Double Sided Doping (DSD). The mobilities measured in the GaAs and InP based NMOSFET structures is higher than typical mobilities in the Si-SiO_2 system by a factor of ≈12 and ≈ 24, respectively.

For sheet carrier concentrations, n_s = 2-3 × 10^{12} cm^{-2} mobilities of 6,000 cm^2/V-s were measured. For higher sheet carrier density of n_s ≈ 6 × 10^{12} cm^{-2}, mobilities of 4,000 cm^2/V-s were measured, with a corresponding sheet resistivity of 280 Ω/sq. Also included in Table 1 is the measured sheet carrier density for the various δ-doping concentrations. Higher sheet carrier density and lower sheet resistivity was observed for the NMOSFET structure compared to the PHEMT structure with the same top and bottom δ-doping concentrations. The trapped surface charge density on the PHEMT structure, under the assumption of surface Fermi-level pinning at 0.7-0.8 eV below the GaAs conduction band edge, was calculated to be 1.0-1.2 × 10^{12} cm^{-2}. From this, the trapped charge density in the oxide is deduced to be as low as 1.5-3.5 × 10^{11} cm^{-2}, which is essential for MOSFET operation.

TABLE I
TRANSPORT DATA

Structure			Transport Data					
Type	δ-Doping (10^{12} cm^{-2})		Electron Mobility (cm^2/Vs)		Sheet Carrier Density n_s (10^{12} cm^{-2})		Sheet Resistivity r_s (W/sq.)	
	Bottom	Top	Mean	σ	Mean	σ	Mean	σ
MOSFET	6	0	6155	120.4	2.42	0.05	422.6	17.9
	6	1	6012	26.1	2.85	0.02	367.1	2.1
	6	2	5303	24.9	3.61	0.05	328.5	4.7
	6	4	4447	3.6	5.03	0.01	280.0	0.5
	6	6	3822	10.7	5.85	0.07	280.3	4.3
PHEMT	6	0	5726	32.7	1.57	0.03	696.2	7.9

CONCLUSIONS

NMOSFET heterostructures employing a high κ-dielectric stack have been grown using molecular beam epitaxy on GaAs and InP susbtrates, and carrier mobilities of 6,000 cm^2/V-s and 12,000 cm^2/V-s (for n_s = 2-3 × 10^{12} cm^{-2}) were measured on the respective substrates. The total oxide charge in the NMOSFET structure was calculated from the measured data to be ≈ 1.5-3.5 × 10^{11} cm^{-2}.

ACKNOWLEDGEMENTS

The authors would like to thank N. England, D. Uebelhoer, and L. Adams for MBE wafer growth and wafer processing, respectively. The support of B. Xie and M. Canonico of the Physical Analysis Lab is acknowledged. Wafer processing has been performed in Motorola's Embedded Systems and Physical Sciences Laboratory. Finally, the authors would like to acknowledge the support of K. Johnson, M. Miller and P. Maniar (Motorola).

REFERENCES

[1] W. Zhu, J.P. Han and T.P. Ma, "Mobility measurement and degradation mechanisms of MOSFET's made with ultrathin high-κ dielectrics", IEEE Trans. Electron Devices, vol. 51, no.1, pp. 98-105, Jan 2004.

[2] The International Technology Roadmap for Semiconductors, 2004 Edition.

[3] M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, R. Gregory, D. Nguyen, "High Mobility NMOSFET Structure with High-k Dielectric," IEEE Electron. Dev. Lett., vol. 26, no. 10, pp. 713-715, 2005.

[4] M. Passlack, "Methodology for Development of High-κ Stacked Gate Dielectrics on III-V Semiconductors," in Materials Fundamentals of Gate Dielectrics," edited by A.A. Demkov and A. Navrotsky, Springer Verlag, 2005, pp. 403-467.

[5] M. Passlack, "Development Methodology for High-k Gate Dielectrics on III-V Semiconductors: $Gd_xGa_{0.4-x}O_{0.6}/Ga_2O_3$ Dielectric Stacks on GaAs," J. Vacuum Science & Technology B, vol. B23, no. 4, pp. 1773-1781, 2005.

[6] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. New York: McGraw Hill, 1975, p.137

ACRONYMS

MBE: Molecular Beam Epitaxy
SSD: Single Side Doping
DSD: Double Side Doping