Reduction of Platinum Metal Usage in GaAs IC Metallization

L. Luu-Henderson, L. Rushing and S. Tiku
Skyworks Solutions, Inc. 2427 W. Hillcrest Dr. Newbury Park, CA. 91320, lam.luu@skyworksinc.com, (805) 480-4339

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Abstract

Ti/Pt/Au is a well established metallization scheme for GaAs IC processing that can be used for the first interconnect layer, FET gate layers, and Schottky contact for diodes. The platinum in this structure is utilized for its properties as a barrier against gold diffusion into the semiconductor, which occurs at processing temperatures above 260°C. Good Schottky diode behavior must be maintained through high temperature processing as well as the life of the circuits. Conventional industry practice for the evaporated Pt layer thickness is to use around 400Å. However, due to the recent rise in the cost of precious metals, it has become important to optimize the thickness of this Pt barrier layer, without jeopardizing device performance and reliability. This paper explores the effect of varying Pt thickness between 0 and 400Å on the electrical stability of Schottky diodes through extended testing at high temperature. Results are encouraging showing that a reduction of Pt may be possible. Reliability testing will continue to further verify the optimum thickness.

INTRODUCTION

The Ti/Pt /Au metallization system has numerous applications in microelectronics. In III-V semiconductor processing it is used for the first interconnect layer, where it may act as the gate layer for FET type devices, Schottky contact for diodes, connect resistors and active devices, and may land on bare GaAs [1]. The metallization must make good mechanical contact and fulfill the electrical requirements. In all these metallization schemes, the basic interconnect metallization is gold. Titanium is used for ensuring good adhesion and Schottky barrier properties. The platinum is used as the barrier metal between gold and titanium. Without Pt, gold migration through Ti can occur into the semiconductor, and Gallium (from GaAs) can diffuse into the gold. Refractory barrier metals like W, Ta and Mo or TiW also provide good barrier properties, but are generally not easily evaporated.

In III-V processing, high temperature operations are avoided after gate layers and Schottky diode contacts are formed. However, a temperature of 300°C is generally required for interconnect processing. The characteristics of the Schottky diode and gates must be maintained through these high temperature steps and circuit-life [2,3,4]. The choice of metals for good Schottky contacts is limited, and is primarily determined by metallurgical compatibility. Fabrication of reliable Schottky diodes is dominated by surface treatments and careful design of the metal stack. As an example, gold and silver make good Schottky barriers on GaAs. However, at temperatures over 260°C, gold diffuses into the contact. This causes metal spiking, barrier height change and deviation from ideality. The Ti/Pt/Au Schottky metal stack is designed to withstand high temperature operation without degradation of electrical characteristics, thus maintaining "ideal" Schottky diode behavior, as shown by the diode ideality factor. The minimum thickness of Pt required is determined by the long term reliability of the device contact or interconnect system, and by solderability of the bond pads. The general tendency in the industry has been to use standard metallization with Ti thickness around 300Å and Pt around 400Å for evaporated metallization. In response to the recent increased cost of precious metals, minimization of the barrier layer thickness while maintaining device performance and reliability has become a crucial focus.

EXPERIMENTAL

The present study was specifically conducted to optimize the Pt thickness needed for Schottky diodes. However, the results should also be applicable to FET Schottky gates. The experimental data was gathered from wafers run on Skyworks standard GaAs production line, using MOCVD grown epi wafers and HBT processing. The Pt thickness was varied from 0 to 400Å at the metal 1 deposition step, which is used as the Schottky contact for the diodes, keeping the rest of the processing standard. A typical diode layout is shown in Figure 1. The area of the diodes was 8μm^2 with n:GaAs doping of 1.0E16-cm^3.

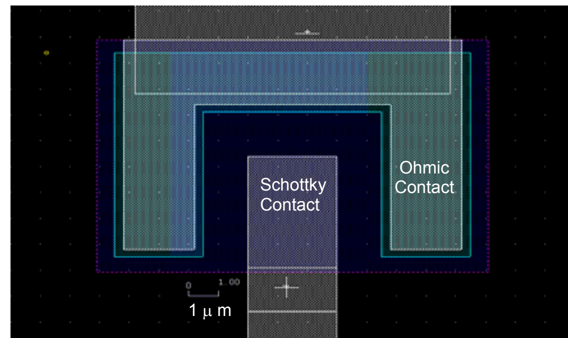

Figure 1. Schottky diode test structure.

Electrical data was gathered from standard PCM test chips, some of which were packaged and bonded for reliability testing. Packaged diodes were subjected to High Temperature Operating Life (HTOL) testing under constant voltage and temperature stress.

To perform the HTOL (High Temperature Operating Life) test, diodes with varying Pt thickness were subjected to constant voltage and temperature stress. This constant stress was chosen for ease of use with the realization that constant current density stress may be used in future testing. If the diodes remain stable, then constant voltage stress equates to constant current density stress.

A stress voltage of 0.6Vwas applied concurrently with a stress temperature of 200°C. At 0.6V, and 200°C, the stress current density is estimated at approximately 37.5µA/µm^2. The zero Pt variant with lower turn on has a much lower stress current density of approximately 8.125µA/µm^2.

During HTOL, the devices were periodically cooled to room temperature in order to perform electrical characterization. Electrical characterization is accomplished by first completing an IV sweep with an HP4155 and then extracting appropriate diode parameters from the IV curves. These parameters are then trended versus time to determine failure times.

The current density-voltage relationship for a Schottky diode under the thermionic emission-diffusion model is given by: [5]

$$Jn = Js \{ \exp(qV/nkT)-1\}$$

where $Js = A^{**} T^2 \{\exp(-q\Phi_{Bn}/kT)\}$ and A^{**} is the effective Richardson constant, k is the Boltzman's constant, q is the electronic charge, Φ_{Bn} is the barrier height, n is the ideality factor and T is the temperature. The diode ideality factor, n and Js can be derived from the slope and intercept determined by plotting the ln[J]-ln[V] data. The ideality factor is then given by:

$$n = (q/nkT)\{ \delta V/\delta (\ln Jn) \}$$

The barrier height Φ_{Bn} can be determined from Js by the following equation:

$$\Phi_{Bn} = kT/q \{ \ln (A^{**} T^2/Js) \}$$

RESULTS & DISCUSSION

The diode stability was checked by measuring diode properties such as the ideality factor and barrier height over an extended reliability study at constant operating voltage and temperature. During any HTOL experiment the fundamental failure mode must be identified. This is best done using IV characterization. Figure 2 and Figure 3 depict the I-V curves taken for the Schottky diodes with zero and 100Å Pt at all read points. The I-V curves for 100Å and 200Å are similar to that of the standard 400Å Pt thickness. Because of this, only results for 100Å Pt thickness are shown in Figure 3 and 5.

The fundamental failure mode for zero Pt variant is a resistive short (with current compliance), as depicted in Figure 2. From Figure 3, the other variants have not exhibited enough degradation to show in the IV curves.

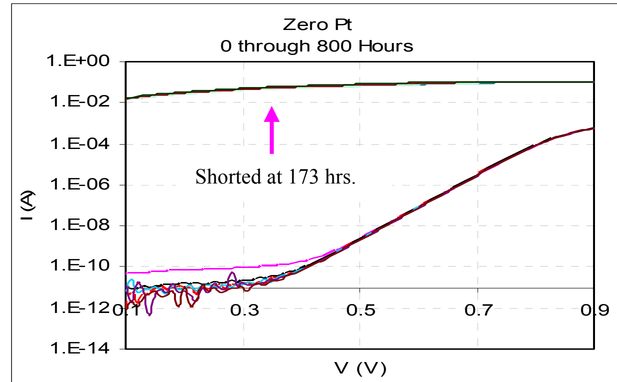

Figure 2. I-V curves for zero Pt Schottky contacts measured at zero and after 800 hours of HTOL showed device failure at173 hours.

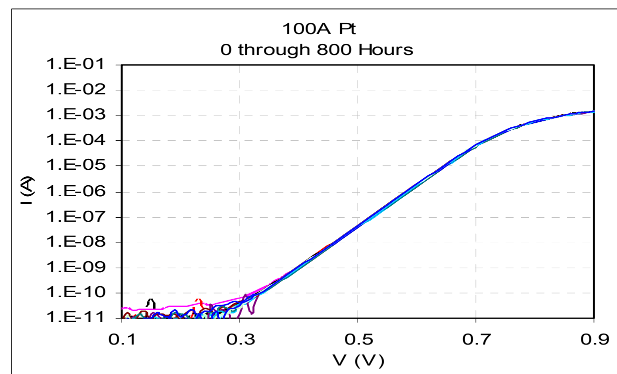

Figure 3. I-V curves for 100Å Pt measured at zero and after 800 hours of HTOL showed stable electrical performance. Curves for 100Å, and 200Å Pt are similar to the standard Pt thickness.

As stated previously, the failure times are analyzed using the parameter trends. The ideality factor for zero Pt thickness as a function of time is shown in Figure 4. This figure shows a systematic population failure at 173 hours.

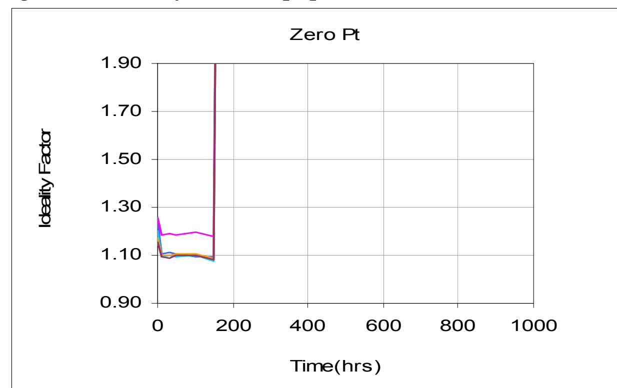

Figure 4. Ideality factor for eight zero Pt Schottky diodes under HTOL exhibiting device failure at 173 hours.

For thicknesses of 100Å and above, minimal degradation is seen (approximately 1.2%), as shown in Figure 5. This is similar to the degradation for the control devices with 400Å Pt Thickness. Thus, the degradation is not attributed to Pt thickness. Once failure occurs the fundamental failure modes can be identified and further conclusions can be made about this 1.2% degradation.

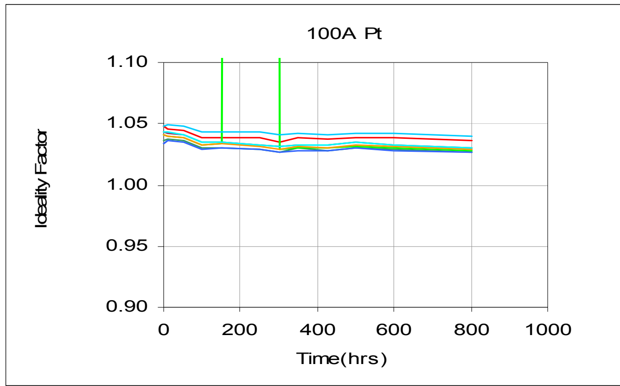

Figure 5. Ideality factor for eight 100Å Pt Schottky diodes at 800 hours of HTOL with minimal device failure.

To compare all variants in a single figure, the data for both the ideality factor and the barrier height are plotted as a function of Pt thickness in Figure 6 and 7. After 173 hours, the zero Pt variants show a clear difference from the rest of the variants for both ideality factor and barrier height. For the 100Å, 200Å, and 400Å variants, the ideality factor is unchanged at 800 stress hours. These data indicate early electrical failure of zero Pt Schottky contact while Pt thicknesses at 100Å and above remained stable after 800 stress hours.

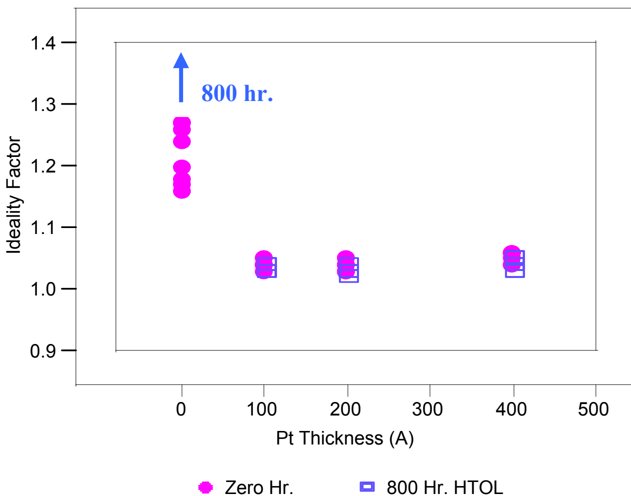

Figure 6. Schottky diode ideality factor dependency on Pt metal thickness at zero and after 800 hours of HTOL exhibiting significant failure for no Pt. Note: ideality factor for zero Pt thickness at 800 hours ranged from 16.9 to 22.6.

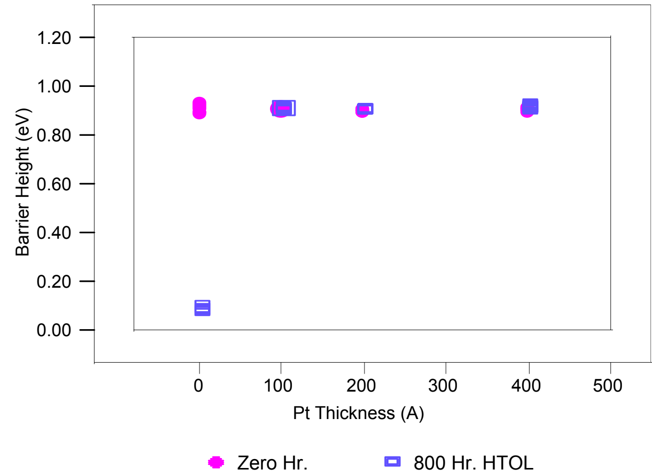

Figure 7. Schottky diode barrier height dependency on Pt metal thickness at zero and after 800 hours of HTOL exhibiting significant failure for no Pt.

The constant ideality factor (close to unity) is a good indicator of thermal stability and offers confidence that there was no gold inter-diffusion. SEM cross sections for each Pt thickness sample were taken on a Focused Ion Beam (FIB) system after 800 hours of HTOL. Inter-diffusion was not evident in the 200Å Pt sample as shown in Figure 8, but gold diffusion at the GaAs–metal interface was noted for the zero Pt sample as seen in Figure 9.

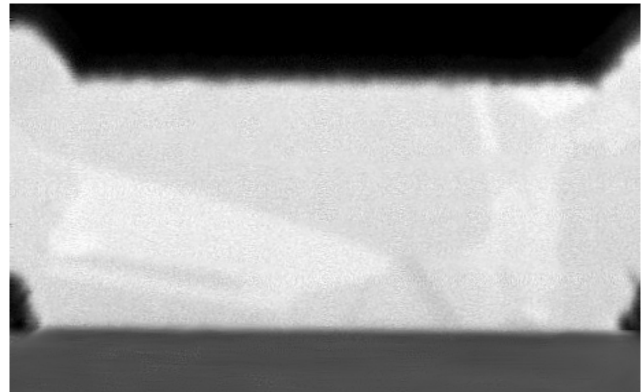

Figure 8. Post HTOL FIB cross section of Schottky diode with 200Å Pt.

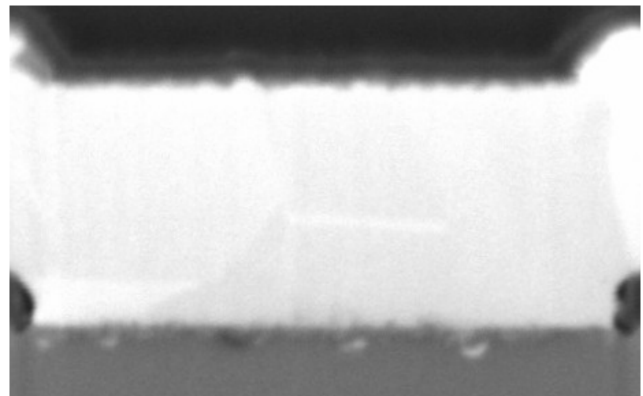

Figure 9. Post HTOL FIB cross section of Schottky diode with zero Pt.

A better detection of metal migration was observed under TEM analysis. [2] Metal diffusion was not visible for the post HTOL 200Å Pt sample as captured in Fig. 10. In contrast, Fig. 11 revealed substantial metal diffusion for the post HTOL sample with zero Pt.

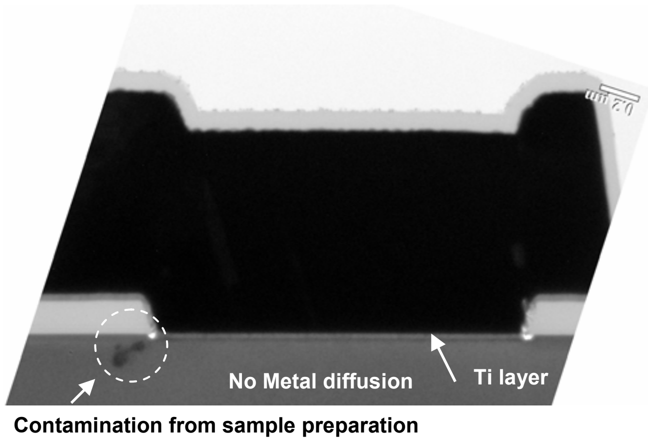

Figure 10. TEM image of sample with 200Å Pt after 800 hr. of HTOL.

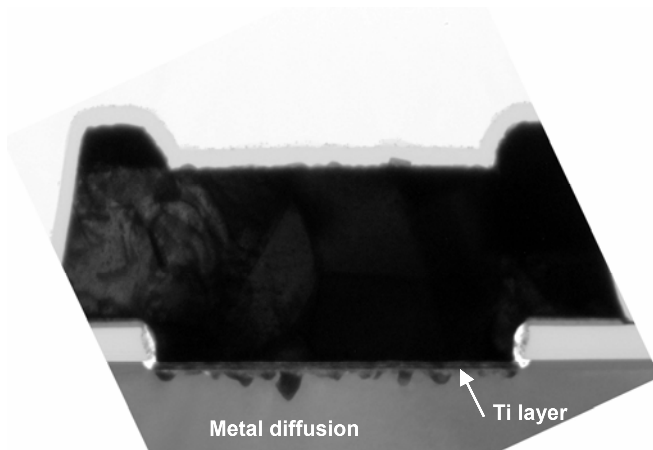

Figure 11. TEM image of sample with zero Pt after 800 hr. of HTOL.

CONCLUSIONS

The Pt layer in the Ti/Pt/Au metallization has a significant role as a diffusion barrier for gold migration in GaAs IC fabrication. Due to the high cost of precious metal, a small reduction in the thickness can translate into a substantial cost saving. Determining the optimal Pt thickness is critical to preserve device characteristics and long term reliability. From considerations of process control, the minimum practical thickness is about 100Å, due to non-uniformity and the possibility of pin holes. Reliability results are encouraging, indicating that thicknesses above 100Å exhibits equivalent performance to the standard 400Å and a thickness of 200Å may be adequate for terrestrial applications. At Skyworks, reliability studies like these are required for feasibility before qualification or implementation is considered. Much more reliability testing would be required prior to process implementation. Reliability testing will continue in order to verify lifetime at stress conditions and predict useful lifetime. Additional work will be pursued for process reproducibility, including multiple lots and understanding of the fundamental reliability physics.

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ACRONYMS

FET: Field-Effect Transistor
HBT: Heterojunction Bipolar Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
HTOL: High Temperature Operating Life
FIB: Focused Ion Beam
TEM: Transmission Electron Microscope