A High Yield Manufacturable BiFET Epitaxial Profile and Process for High Volume Production

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Abstract

The integration of FET in the conventional GaAs HBT process (BiFET) has provided an additional degree of freedom in the design of advance bias circuits in GaAs Power Amplifier and Analog/Mixed Signal applications. This paper discusses the development of a GaAs based BiFET technology, including the epitaxial profile and process controls to achieve high fab yield and manufacturability. Epitaxial profile that integrates an HBT and a MESFET on the same GaAs substrate and Capacitance-Voltage profiling for quality control are discussed. Influence of various fabrication process steps on FET parameters and the process optimization steps are presented. Through such careful process control procedures, high DC probe yield for the BiFET designs has been demonstrated.

INTRODUCTION

The integration of III-V Hetero-junction Bipolar Transistors (HBT) and Field Effect Transistors (FET), often termed as BiFET, has attracted significant attention due to the possibilities of advanced bias circuit designs such as bias enable switch, stage bypassing and adaptive gate switching, lower/no reference voltage and analog controls in the design of linear power amplifiers [1, 2]. Several BiFET integration schemes have been proposed and demonstrated by other research groups. These various schemes include re-growth (selective area, or pre-patterned multilayer growth) [3, 4], two-step growth (stacked devices) [5], and merged growth (single growth has both devices and the devices share layers) [6]. To establish a BiFET process in our high volume GaAs HBT production line, we have evaluated some of these possible BiFET integration approaches and found most of these methods having drawbacks with respect to high volume manufacturing. Due to our stringent yield requirement in a cost conscious environment, a merged BiFET approach was selected and developed.

In this paper we discuss the considerations and the development process for a merged BiFET epitaxial profile with an etch stop layer. Quality control metrics for the incoming epitaxial material as well as fabricated HBT and FET devices are developed. Critical process modules that influence the FET performance and their optimization are discussed. Device reliability and BiFET product probe yield data are presented at the end.

MATERIAL GROWTH AND DEVICE FABRICATION

The epitaxial layers, comprising of InGaP emitter, base and collector of the HBT, are grown on SI GaAs (100), by using MOCVD technique. The FET specific layers such as channel and an optimized etch stop layer are grown within the emitter of the HBT. A schematic cross sectional profile of the BiFET layer scheme is shown in Figure 1.

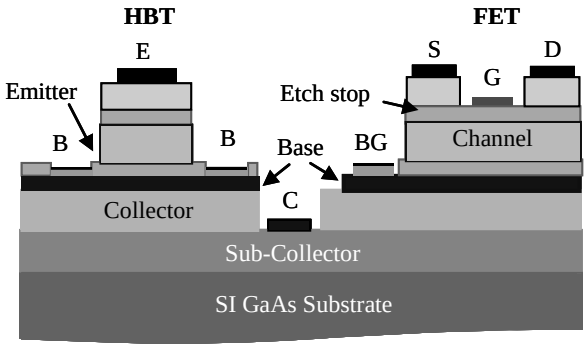

Figure 1: Schematic cross section of an integrated HBT and FET. S, D, G, BG are the source, drain, gate and back-gate contacts of the FET and E, B, C are emitter, base, and collector contacts of the HBT respectively.

In a high-volume GaAs HBT manufacturing environment, the starting epitaxial materials should be "pre-screened" and sufficient quantities need to be kept in material inventory or in consignment for uninterrupted lot starts. A "quick-lot" (QL) process is often used by material suppliers to ensure that the incoming HBT wafers meet desired specifications. Typically, large area (75μm x 75μm) HBT devices are fabricated and electrical parameters such as DC gain, offset voltage, base-emitter/base-collector turn-on voltages, sheet resistances, and junction breakdown voltages are measured from multiple sites on a witness wafer. However, since FET devices are sensitive to process conditions, electrical measurements such as pinch off voltage, saturation current and transconductance vary significantly due to process and mask the growth variations. Hence, the FET QL process and electrical characterization of FET are often inadequate to screen the quality of the FETs.

In addition, an alternate FET QL procedure should also be simple to interpret, faster and depend only on the run-to-run and machine-to-machine growth variations. To this end, in collaboration with the epi supplier, a Capacitance-Voltage (C-V) based QL procedure has been established. Figure 2 illustrates a typical emitter-base junction C-V profile collected from a set of DOE (design of experiments) wafers with different doping concentrations. From the C-V profile, one can extract the FET channel thickness and doping concentration, as depicted in Figure 2. Using this simple characterization technique, consistent thickness and doping information have been obtained to establish correlation with the FET electrical parameters that are acquired after full wafer fabrication. Failure to implement such QL strategy can result in very costly yield issues and potential scraps at the end of line.

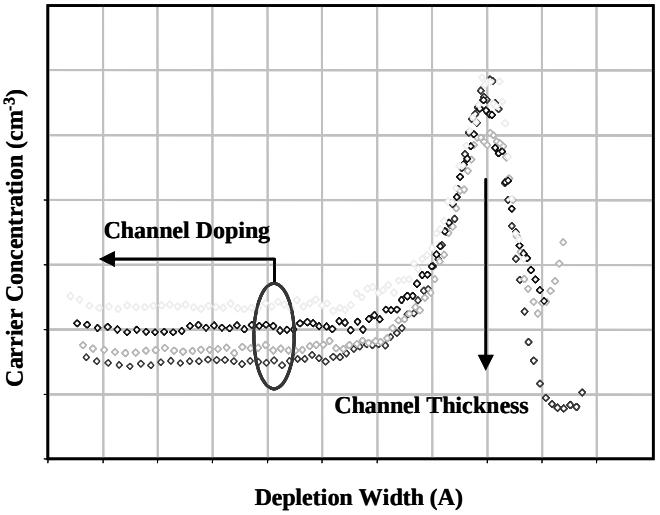

Figure 2: C-V profile of Emitter-Base in a BiFET wafer. Different curves are collected from a set of DOE wafers with different doping concentrations.

BiFET fabrication is carried out in Skyworks' high volume HBT manufacturing line. Dry etch processes are used to define emitter and base opening of the HBT and wet etch process is used to define the collector opening. Appropriate contact metals and associated annealing schemes are used to fabricate ohmic contacts to the HBT device. He^{++} ion implantation is used for device isolation. In defining the FET, challenge is to add minimum number of masking steps to define the channel and gate regions and these FET specific process steps have to be introduced in the HBT flow at the appropriate steps and still preserve the electrical integrity of the FET and HBT devices. Source and Drain contacts of the FET share the same fabrication steps that are used to form the emitter contacts of the HBTs. In placing the gate metallization step, care should be taken to limit the exposure of gate metal Schottky contact to high temperatures (>300 deg C) and longer isothermal anneal cycles. FET device-to-device isolation is achieved by the combination of dry etch and ion implantation process, both of which are used in the definition of the HBTs.

INFLUENCE OF FABRICATION STEPS ON FET

To achieve the goal of high FET yield, similar to that of HBT, a process must meet the following criteria:

- Pre-screened incoming epitaxial wafer from the material supplier
- Optimized FET device layout for low Source-to-Drain leakage
- Low resistance ohmic contacts for the Source and Drain
- Precise control of the channel etch process
- Consistent Gate definition process with tight control of gate length and the quality of Schottky gate metal interface
- Optimized annealing steps and controlled thermal budget to avoid gate metal diffusion
- Set of Process Control Monitors (PCM), to monitor the consistency of the FET parameters as well as to troubleshoot and isolate the problematic step in the flow in case of epi/process/tool issues.
- Setting the upper (UCL) and lower (LCL) control limits for FET DC parameters, that are validated through circuit performance.
- Facilitate the DC probing of the FETs (directly or indirectly) in the design (design for testability) to accurately define the GYDPW (Gross Yielding Dies per Wafer) prior to the assembly process.

Epitaxial Variation

The implication of run-to-run growth variation on the C-V profile and the correlation to FET pinch off voltage is shown in Figure 3 and Figure 4. From the C-V profile, one can infer that the bulk channel doping and channel thickness of the two groups of wafer are the same.

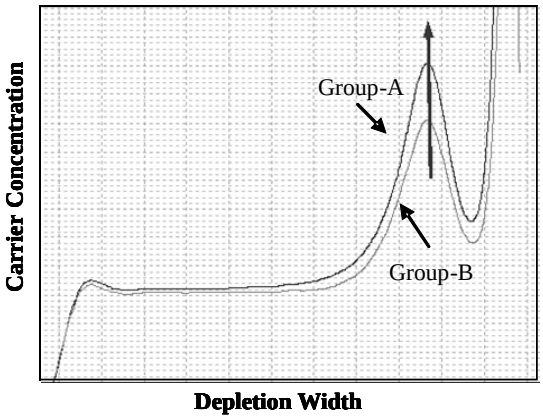

Figure 3: C-V profiles of Emitter-Base of BiFET wafers. Group-A and Group-B wafers come from different MOCVD growth runs.

However, the charge difference between the runs, as shown in Figure 3, could be the result of either charge build-up at the interface of etch-stop layer and the channel layer and/or the doping in the etch-stop layer, which results in a shift of 100 mV in the pinch off voltage, as shown in Figure 4.

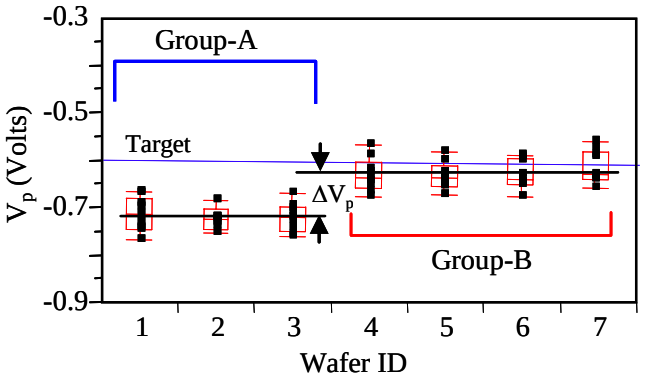

Figure 4: Pinch off voltage Vs Wafer ID of a depletion mode FET from a single fabrication run. Note the ΔV_p of 100 mV between two groups arise due to difference in epitaxial layers resulting.

Gate Definition Process

The metal-semiconductor FET in the BiFET technology consists of a thin etch stop layer between the e-beam evaporated Ti/Pt/Au/Ti Schottky gate electrode and the GaAs channel layer. In this structure, the gate-metal/Etch stop layer Schottky contact is the key component, though these Schottky contacts are not intimate metal semiconductor contacts, and is separated by a thin inadvertent interfacial layer formed due to cross-diffusion, out-diffusion and chemical reaction between metal and semiconductor. It is, therefore, critical to optimize the gate definition process steps which prepare the surface consistently prior to gate metallization. Several wet (NH4OH vs. HCl cleaned) and plasma surface passivation (O2, SF6) processes are investigated. The ideality factor, $n = (q/k_BT)(dV_{gs}/d\ln I_g)$ is determined from the forward I-V characteristics of the Gate, at 300K. Change in ideality factor as a function of applied voltage, as illustrated in Figure 5, is used to determine the quality of the metal-semiconductor contact. Curve (a) in Figure 5 is collected from a FET, fabricated with an optimized gate process, while curve (b) in Figure 5 is collected from a FET with the pinch off voltage of -0.2V and the saturation current was dropped by more than 10 times of the target value. For a good metal-semiconductor Schottky contact, with no inter-diffusion of Ti or Ga out diffusion, the ideality factor at $Vg \leq 0.4V$, where thermionic emission is dominant, is 1.23, which correlates well with the reported value [7]. For an imperfect Schottky contact (Figure 5b), the ideality factor increases with bias to almost 5, and then decreases. Such voltage dependence of n is very unique in III-V semiconductors with high density of surface states. Surface imperfections and sinking gate, leading to the distribution of interface states in the forbidden gap, are the major cause of non-ideal behavior in Schottky contacts [8-9], and are revealed by the TEM (Transmission Electron Microscopy) of the gate region, as shown in Figure 6.

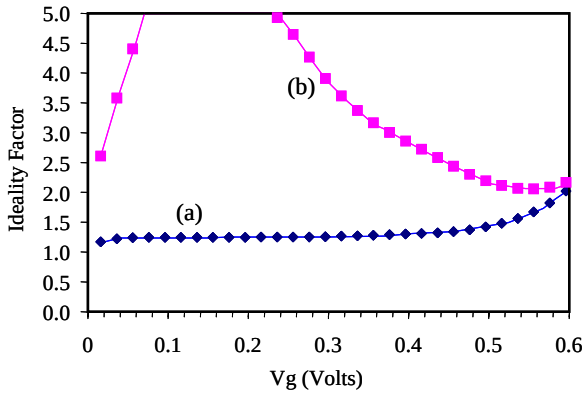

Figure 5: Ideality factor as a function of gate voltage of the Schottky contact. Curve (a) is generated from a FET with good electrical characteristics and curve (b) is generated from a FET with poor electrical characteristics.

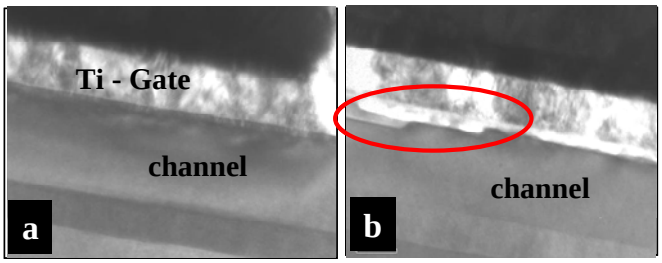

Figure 6: Transmission Electron Micrographs of the Gate region. Image (a) is from the gate Schottky with n=1.23 and image (b) is from the non-ideal Schottky contact with n>2. Note the sinking gate, highlighted in image (b).

MANUFACTURABILITY

In addition to establishing the control procedures for the incoming epitaxial material, each process modules in the fabrication steps were carefully optimized. The process capability (Cp, Cpk) were assessed from the electrical parameters of both HBT and FET devices and the statistical data was used for circuit designs. Besides process control procedures, it is also critical that the FETs in the BiFET circuits should be probable, either directly or indirectly, in order to accurately calculate the gross yielding dies per wafer. For example, indirect measurement in the bias enable path could be simply toggling the FET and measuring the base voltage to the amplifier in the FET on-state and bias leakage in the FET off-state. Extensive test coverage during the early stage in high volume manufacturing will identify possible epitaxial material, process and/or tool issues. As a result, high DC probe yield in CDMA and WLAN products based on BiFET technology, comparable to the HBT only based products, have been achieved, and are depicted in Figure 7.

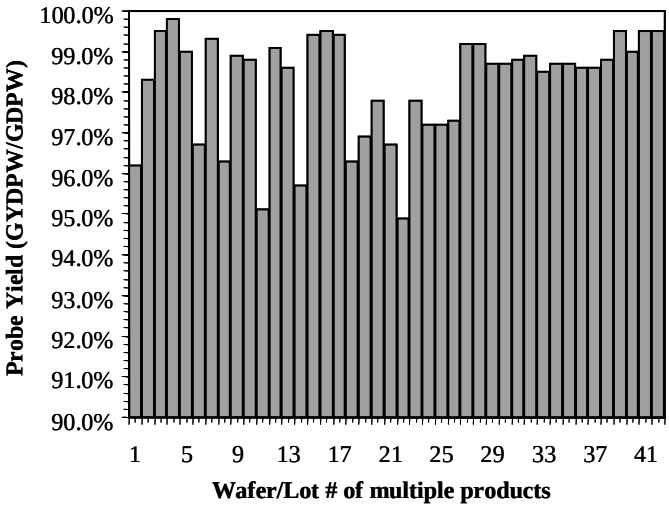

Figure 7: DC probe yield as a function of wafer/lot numbers collected over time. Gross Yielding Dies per Wafer is computed after performing a series of DC tests for both HBT and FET active devices as well as passives such as resistors, and capacitors in the design.

CONCLUSIONS

Importance of screening incoming epitaxial material has been shown to be crucial for achieving/maintaining high yield in the manufacturing. To this end, Capacitance-Voltage characterization method was used to qualify the FET specific layers, along with the electrical characterization of HBTs using large area processing, in the BiFET wafers. The sensitivity of C-V method was found to be adequate to quantify growth run-to-run variations and good correlation has been made to the FET electrical parameters at the end of line. Bias dependant ideality factor n and decrease in transconductance g_m as a function of different process steps were studied and optimized process conditions were chosen such that there is no degradation to the FETs and HBTs in the BiFET technology. With the implementation of stringent control procedures as well as circuit validated control limits, high probe yield in the BiFET based circuits has been demonstrated.

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ACRONYMS

HBT	: Hetero-junction Bipolar Transistor
FET	: Field Effect Transistor
MOCVD	: Metal Organic Chemical Vapor Deposition
BiFET	: Merged HBT and FET device
DOE	: Design of Experiment
GDPW	: Gross Dies Per Wafer
GYDPW	: Gross Yielding Dies Per Wafer