InGaP-*Plus*™: A Low Cost Manufacturable GaAs BiFET Process Technology

Mohsen Shokrani, Kezhou Xie, Boris Gedzberg, Wojciech Krystek,
Prabhu Mushini, Aditya Gupta, Pat Fowler, William Peatman

ANADIGICS, Inc., 141 Mount Bethel Road, Warren, NJ 07059, USA
mshokrani@anadigics.com; (908) 668-5000

Keyword: BiFET, integration, InGaP, HBT, pHEMT, manufacturable

Abstract

InGaP-*Plus*™ technology (patent pending), a low cost manufacturable GaAs BiFET process has been developed at ANADIGICS for high volume production of commercial MMICs. A vertically integrated HBT and pHEMT epitaxial structure has been designed to allow complete decoupling of HBT and pHEMT device structures. This enables independent optimization and development of each device to achieve the required performance without any compromises. The process flow has been developed to maximize the number of shared fabrication steps to minimize cost and maximize yield. The extensive DC and RF characterization show that HBT and pHEMT devices in the BiFET wafer have the same performance and reliability as the stand-alone HBT and pHEMT devices. The process control data for over one year of production demonstrate a stable InGaP-*Plus*™ process with good process capability.

Introduction

InGaP HBT technology has been widely used in many commercial applications such as wireless handsets and wireless LAN for its many unique advantages. The constant requirement of additional product functionality, performance and integration and reduction in product size and cost demands a better HBT technology. Monolithic integration of HBT and pHEMT on the same chip offers many advantages such as design flexibility for higher levels of circuit function integration and improved performance while reducing product cost and size. Silicon industry has achieved this and benefited from the BiCMOS technology for many years. Attempts to Integrate GaAs based HBT with FET devices have been reported in the literature [1-4]. However, these approaches suffer various shortcomings, such as limited FET performance due to the constraint of the layers shared by HBT and FET or complicated and costly epi re-growth. So far integration of such devices in the GaAs industry for high volume manufacturing of commercial products with low cost and high yield has not been demonstrated. In this paper we report the development and high volume manufacturing results of a monolithically integrated InGaP HBT and AlGaAs pHEMT structure on the same substrate (InGaP-*Plus*™).

InGaP-*Plus*™ Epi Structure

To minimize development effort and qualification cost, the existing stand-alone production HBT and pHEMT device structures were chosen for monolithic integration with minimal changes. The basic concept of the integrated pHEMT/HBT structure is shown schematically in figure 1. In this vertical integration approach, the pHEMT layer structure is epitaxially grown first on the substrate and the HBT layer structure is grown atop the pHEMT layers. This is achieved in one uninterrupted epi growth run. In this structure, HBT and pHEMT only share a highly doped n-type GaAs layer that serves as the cap for pHEMT and as the sub-collector for HBT. The thickness of this layer should be chosen to achieve the required HBT collector resistance while maintaining acceptable pHEMT recess topography to allow pHEMT gate processing and formation. The optimal subcollector thickness can be determined through physical device simulation and circuit testing. This approach completely de-couples the active device layers of HBT and pHEMT. Furthermore, pHEMT and HBT in this structure

can be independently optimized to achieve the required performance objectives for different circuit applications with good manufacturing margin.

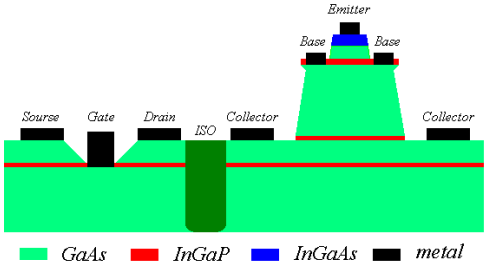

Figure 1. Schematic cross section of the integrated HBT and pHEMT in InGaP-*Plus*™ technology.

The ANADIGICS InGaP-*Plus*™ wafers are grown by MOCVD technique. First, a buffer layer structure consisting of GaAs/AlGaAs layers optimized for low leakage and optimum pHEMT device characteristics is grown on the substrate. The double delta doped pHEMT structure consisting of a lower barrier layer, an InGaAs channel and an AlGaAs Schottky barrier layer is grown next. An InGaP etch stop layer is grown on top of the AlGaAs Schottky barrier layer for recess etch control.

After completion of pHEMT layers, a highly doped GaAs contact n-layer with optimum thickness is grown on top of the etch-stop layer and serves as the cap layer of pHEMT and the subcollector layer of the HBT. The rest of the InGaP HBT structure layers are grown next. An n-type collector is grown on top of the subcollector followed by a p-type GaAs base layer and an n^- InGaP emitter layer. A highly doped InGaAs is grown as emitter contact layer.

InGaP-*Plus*™ Fabrication Process

The InGaP-*Plus*™ process flow consists of three process modules: HBT, pHEMT and passives and interconnects. Since the intrinsic HBT and pHEMT process modules are independent of each other, they can be separately modified to accommodate different HBT and pHEMT structures. The InGaP-*Plus*™ process was developed using the existing well-established production process modules with some modifications and did not require new equipment procurement. This allowed us to keep the development cost low and development time short.

The major InGaP-*Plus*™ process steps are as follows. The process begins by formation of the emitter ohmic contact using evaporation and lift-off. Emitter mesa is defined using photoresist mask and selective wet etch of the emitter cap. Next, the base ohmic contact is formed by selective wet etch of InGaP emitter layer and evaporated metal lift-off. Base mesa is defined next by selective wet etching of the collector layer using photoresist mask. The preceding process steps are specific to the formation of the HBT.

A nitride passivation layer is deposited by PECVD on the wafer to protect the HBT device during subsequent process steps. Helium ion implantation is used to provide electrical isolation between HBTs, pHEMTs and other active and passive devices. The isolation implant profile is designed to isolate the pHEMT layers including the highly doped n-layer cap. The isolation resistance achieved in the InGaP-*Plus*™ process is similar to the stand-alone HBT process with no degradation. After the isolation step, the collector ohmic contact of the HBT and the source/drain ohmic contact of the pHEMT are formed in one step using standard AuGe/Ni metalization and alloy. At this point the intrinsic HBT device fabrication is completed.

The next two process steps are specific to intrinsic pHEMT device fabrication. The pHEMT recess area is defined by photoresist and selective wet etching. The pHEMT gate formation process depends on the specific device structure and required application. The gate metal of the pHEMT described in this paper is formed by metal evaporation and lift-off. Optimum photoresist thickness is required for the recess and gate layers to ensure sufficient step coverage of the HBT structures while achieving the required resolution. After the gate formation, the wafers are passivated with a PECVD deposited silicon nitride film completing the intrinsic pHEMT device fabrication.

The remaining process steps are to form MIM capacitors, inductors, NiCr resistors and interconnect metals and final passivation. Upon completion of the frontside processing, the wafer goes through the standard backside via process and die separation.

InGaP-*Plus*™ Performance and Reliability

The InGaP-*Plus*™ HBT and pHEMT devices were extensively characterized for performance and reliability and the results were compared to the devices fabricated with the stand-alone process. The main items to be addressed were to prove that the integrated Epitaxial growth and fab processing has not degraded the individual device performances and reliability.

DC and RF characterization of discrete HBTs shows no degradation in performance. Comparison of HBT product circuit performance fabricated in the InGaP-*Plus*™ technology and stand-alone process also showed similar performance. The transfer curves and I-V characteristics of

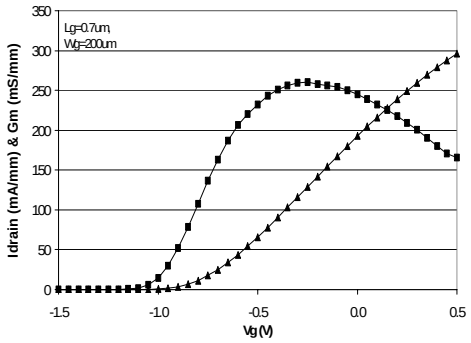

Figure 2. Transfer curves of pHEMT with 0.7 um gate length and 200 um gate width at Vd=3V.

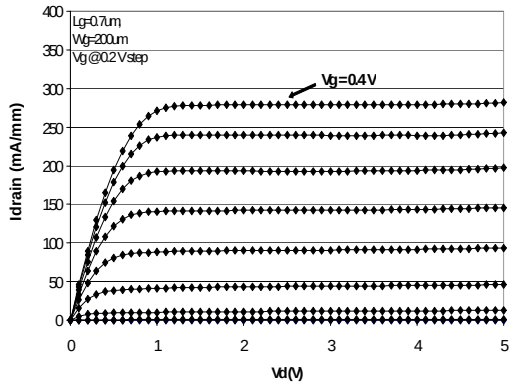

Figure 3. I-V curves of pHEMT with 0.7 um gate length and 200 um gate width at Vg=0.2V per step.

pHEMT with 0.7 um gate length are shown in Figs. 2 and 3. Both DC and RF testing indicate that there is no degradation in the pHEMT performance. Of course, the pHEMT and/or HBT parameters can be altered to meet the particular product application requirements by changing the epi structure design without affecting each other since they are de-coupled in the InGaP-*Plus*™ technology.

InGaP-*Plus*™ HBT reliability is determined by the activation energy (Ea) and Mean Time To Failure (MTTF) through high temperature operating life (HTOL) test. The tests are carried out at three junction temperatures of 250°C, 285°C and 320°C with junction current density at 25kA/cm^2 and Vce = 3.3 V. As shown in Fig. 4, Ea and MTTF of the InGaP-*Plus*™ HBT are found to be 1.2 eV and 2x10^7 hrs, respectively, indicating no degradation compared to the stand-alone HBT. InGaP-*Plus*™ pHEMT reliability is tested at full Idss at a junction temperature of 210°C under drain voltage of 3 V. No significant degradation in Idss is observed after 1000 hours of testing as shown in Fig.5. This result establishes the pHEMT reliability. It is concluded that InGaP-*Plus*™ HBT and pHEMT device performance and reliability is not degraded.

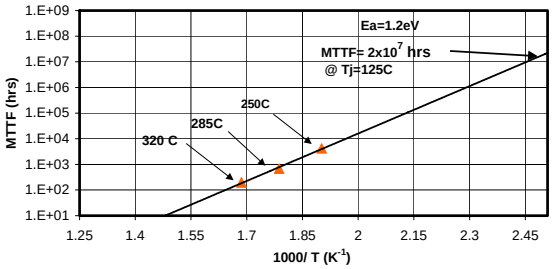

Figure 4. MTTF of HBT as a function of inverse junction temperature

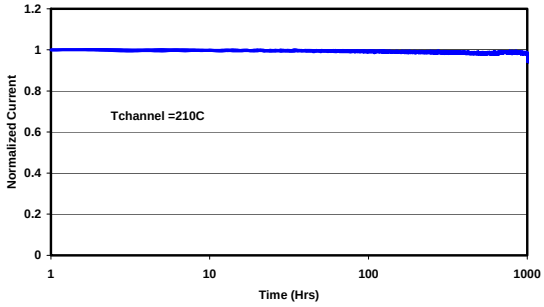

Figure 5. Full Idss reliability of pHEMT at Vd=3V and Vg=0.V.

InGaP-*Plus*™ Volume Production

The device parametric control and yield of the InGaP-*Plus*™ process technology is also of

interest. To ensure good parametric control, the incoming epi wafers as well as key process parameters have to be very tightly controlled. A close working relationship with the epi vendor has been established. Correlations between key final device parameters and epi parameters measured at the vendor site such as HBT and pHEMT quick fab and Hall measurements have been established. These correlations have allowed ANADIGICS to establish the necessary high yields for high volume and low cost commercial product applications. Furthermore, all critical in-line and PCM parameters are monitored using real time Statistical Process Control (SPC) with well defined specification limits based on correlations to device and product performance requirements. With the successful transfer of this process technology to high volume manufacturing, ANADIGICS has successfully produced thousands of InGaP-*Plus*™ wafers with good yield and control. The process capability of InGaP-*Plus*™ process is similar to that of the stand-alone HBT and pHEMT processes. Fig. 6 and 7 show trend charts of normalized HBT DC gain and pHEMT IDss, respectively, for over 1 year of production runs.

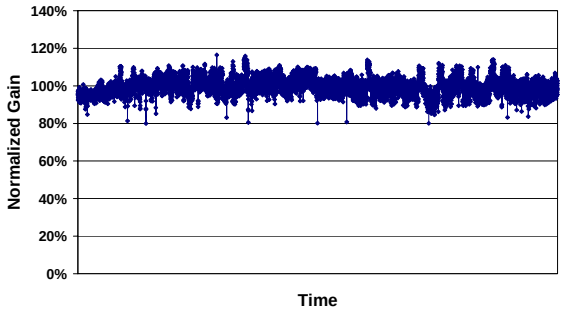

Figure 6. Trend chart of HBT DC Gain

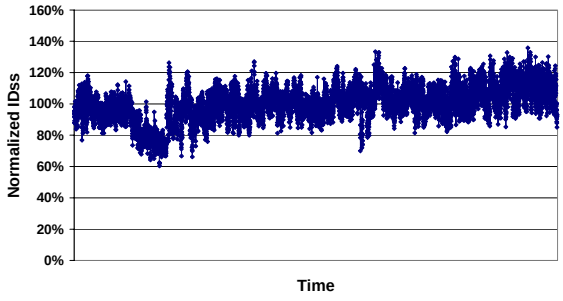

Figure 7. Trend chart of pHEMT IDss

Conclusion

InGaP-*Plus*™, a GaAs BiFET process technology has been developed at ANADIGICS. The epi design allows for a low cost and manufacturable process and provides flexibility in independently optimizing each device. It is shown that the BiFET HBT and pHEMT have the same performance and reliability as stand-alone HBT and pHEMT technology. High volume manufacturing of InGaP-*Plus*™ wafers with good process control have been demonstrated.

Aknowledgment

The authors would like to acknowledge the contribution and support of various groups to this work at ANADIGICS including Technology Development, Manufacturing and Product segments.

.

References

1. W.J. Ho, M.F. Chang, S.M. Beccue, P.J. Zampardi, J. Yu, A. Sailer, R.L. Pierson, K.C. Wang, “A GaAs BiFET LSI technology”, *GaAs IC Sym. Tech. Dig.*, 1994, p.47.
2. D. Cheskis, C. E. Chang, W. H. Ku, P. M. Asbeck, M.F. Chang, R.L. Pierson, S. Sailer, “ Co-integration of GaAlAs/GaAs HBT’s and GaAs FET’s with a simple manufacturable process”, *IEDM Tech. Dig.*, 1992, p. 91.
3. D. C. Streit, D. K. Umemoto, K. W. Kobayashi, A. K. Oki, “Monolithic HEMT-HBT integration by selective MBE”. *IEEE Trans. Electron Devices*, vol. 42, 1995, p.618.
4. D. C. Streit, D. K. Umemoto, J. R. Velebir, K. W. Kobayashi, A. K. Oki, “35 GHz HEMT amplifiers fabricated using integration HEMT-HBT material grown by selective MBE”, IEEE Microwave Guided Wave Lett., vol. 4, 1994, p.361.