Investigation of Base-Collector Parasitics For Various Emitter and Base Geometries in GaAsSb/InP Type-II DHBTs

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Abstract: GaAsSb/InP type-II DHBT transistors have been fabricated using a number of different base geometries. The devices have been modeled and their small signal parasitic components have been extracted. This work will examine the effects of having a realigned base, then compare different geometries and show why the current power transistor design is not conducive towards high speed applications.

1. Introduction

The current InP HBT device results continues to achieve record speed results. A new class of HBT devices, known as the pseudomorphic HBT (PHBT), which is similar to an InGaAs/InP SHBT, has achieved world record results with f_T = 710 GHz while maintaining a respectable f_{MAX} = 340 GHz and a BV_{CEO} = 1.7V [1]. For more robust applications, the InGaAs/InP DHBT has demonstrated simultaneous f_T and f_{MAX} over 300 GHz using a manufacturable technology [2] with a BV_{CEO} over 4V. The InGaAs/InP double heterojunction HBT (DHBT) is a reasonable technology for high speed, moderate voltage applications.

One major limitation of the InGaAs/InP DHBT technology is the type-I conduction band at the base-collector junction. This discontinuity requires complex grading schemes at the base-collector junction to diffuse the potential barrier. The grading typically involves the insertion of an InGaAs and an InGaAsP layer, resulting in a reduction in BV_{CEO} compared with an all-InP collector. This effect becomes more pronounced as the collector is scaled, which is necessary for higher speeds. As the collector is scaled, the distinction between the InGaAs/InP DHBT and SHBT becomes reduced, as seen in figure 1.

One alternative to the InGaAs/InP material system that can achieve both high speeds and while maintaining its breakdown voltage advantage over an SHBT is the GaAsSb/InP DHBT material system. It has a type-II conduction band at the base-collector junction, negating the

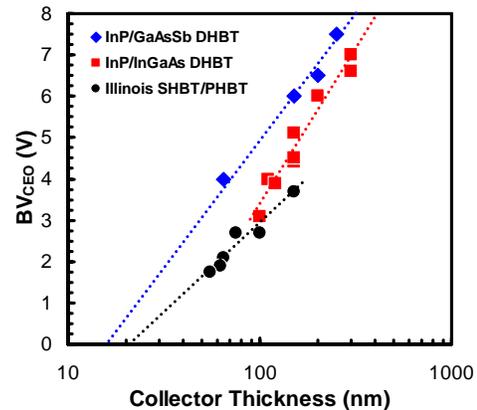necessity for grading. This allows the GaAsSb/InP material system to aggressively scale its all InP collector.

Fig. 1: BV_{CEO} vs. collector thickness for the different InP HBT material systems. As the collector is scaled, the InGaAs/InP DHBT loses its advantage over the InGaAs/InP SHBT, while the GaAsSb/InP DHBT maintains its advantage.

The promise of the GaAsSb/InP material system has been demonstrated in recent years. Simon Frasier University demonstrated the ability of this material system to compete with its InGaAs complement, reporting f_T > 300 GHz and a Johnson Limit > 1800 GHz-V [3]. Recently, further progress in both vertical scaling and material engineering has allowed the InP/GaAsSb material system to achieve an f_T > 472 GHz while maintaining a BV_{CEO} of 4V [4].

The ability to achieve high speeds with high BV_{CEO} makes the device ideal for high-speed, moderate power applications. However, since the conventional layout of the transistor sacrifices reduction of parasitics for yield, specifically the base resistance and the base-collector capacitance, it is inadequate for high-speed applications. This work examines three different transistor layouts to determine their effectiveness in controlling unnecessary the

extrinsic base resistance and eliminating extrinsic base-collector capacitance.

2. Layer Structure and Device Fabrication

Three different layer structures were used to investigate three transistor geometries in this study. The layer structures were designed as follows. Layer structure one consisted of a 25 nm, strained $GaAs_{0.65}Sb_{0.35}$ base, C-doped to 6e19 cm^{-3} and a 75 nm InP collector unintentionally doped. Layer structure two consisted of a 40 nm, lattice-matched $GaAs_{0.51}Sb_{0.49}$ base, C-doped to 4.5e19 cm^{-3} and a 200 nm InP collector, Si-doped to 3e16 cm^{-3}. The final structure consisted of a 40 nm lattice-matched $GaAs_{0.51}Sb_{0.49}$ base, C-doped to 4.5e19 cm^{-3} and a 200 nm InP collector, Si-doped to 3e16 cm^{-3}. The difference between the second and the third structures are a slight doping difference in the emitter.

Geometry A was a structure that sacrifices yield for control over parasitics. The fabrication, described in detail in [5], used an emitter contact defined by electron beam lithography. The self-aligned base contact was also defined by electron beam lithography. The collector contact was defined by optical lithography. The emitter and base mesas were created using a self-aligned, selective wet etch process. That is, the emitter and base metals acted as masks for the emitter and collector etches. The extrinsic base-collector capacitance associated with the base contact was eliminated by undercutting a metal μ-bridge that connects the base contact to the intrinsic emitter. Due to the self-aligned base, the base resistance is reduced, while the isolated base contact minimizes the extrinsic base-collector capacitance. Geometry A was designed to minimize any extrinsic capacitances. An SEM view of this device is shown in figure 2a.

Geometry B was similar to the first except that instead of self-aligned base metal, this device utilized a 0.15 μm emitter-base realignment to eliminate emitter-base shorts. This device allows the effect of a small realignment to be seen in device performance. An SEM view of this device is shown in figure 2b.

Geometry C was a power transistor in the typical wishbone form. An SEM view of this device is shown in figure 2c. The emitter, base, and collector metals were all defined by optical lithography. The mesas were defined by the same etch process used for the first structure. The base metal and collector etch were realigned and there is no isolation of the base contact. In addition this study also compares a one-fingered device with the wishbone geometry to a four-fingered device.
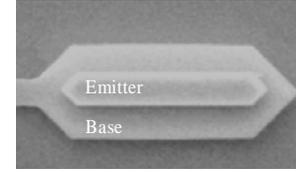
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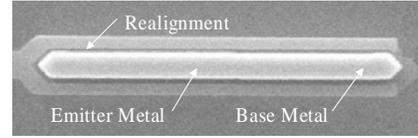
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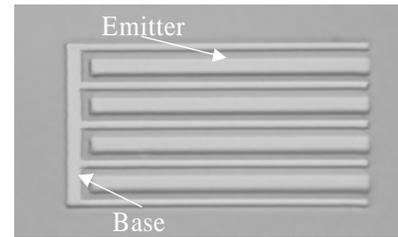
(c)

Fig. 2: Top down views of transistors fabricated using a) geometry A, a transistor with an isolated base contact and a self-aligned base metal, b) geometry B, with a realigned base metal and an isolated base contact, and c) geometry C, a typical power transistor using multiple fingers, a realigned base metal, and a non-isolated base contact.

Layer structure one was used to investigate geometries A and B. Layer structures two and three were used to compare geometries A and C. The layer structures and corresponding geometries are summarized in table 1.

Table 1: Base and collector designs for structures 1, 2, and 3.

Material	Structure 1	Structure 2	Structure 3*
GaAsSb (base)	25nm, C=6e19	40nm, C=4.5e19	40nm, C=4.5e19
InP (collector)	75nm, Si=1e16	200, Si=3e16	200, Si=3e16

*- The difference between structures 2 and 3 is a slight difference in the emitter doping.

S-parameters were taken with an HP8510C network analyzer, sweeping from 500 MHz to 50 GHz. The calibration used was a standard on-wafer SOLT calibration with f_T and f_{MAX} values extrapolated using a –20dB/decade extrapolation between 35 and 50 GHz. The C_{BC} was calculated from S-parameters as described in [6], while R_B was calculated from geometry.

3. Results and Discussion

The modeled, small signal R_B and C_{BC} values, calculated from S-parameters, are shown in table 2. As expected, geometry A has the lowest parasitic values and highest f_T and f_{MAX} values when compared to the other two geometries. Additionally, the effects of the geometry has a much larger effect on f_{MAX} than f_T. This is due to the larger dependence

Base Design	Structure Used	Emitter Size (μm^2)	f_T (GHz)	f_{MAX} (GHz)	R_B (Ohms)	C_{BCi} (fF)
A	1	0.35x8	353	231	35	19.9
B	1	0.35x8	325	157	51	22.9
A	2	2x8	81	77	64.3	30.4
C	3	2x10	101	60	107.8	78
C	3	4 finger, 2x10	80	46	109.1	215

Table 2: Summary of the which the performance of each base design, the structure used to investigate them, and the corresponding parasitic values

of f_{MAX} on parasitics than f_T, as shown in equations (1) and (2).

$$\frac{1}{2\pi\, f_T} = \tau_B + \tau_C + \frac{kT}{I_C}C_{je} + (R_C + R_E + \frac{kT}{I_C})C_{BC} \quad (1)$$

$$f_{MAX} = \sqrt{\frac{f_t}{8\pi\, R_B C_{BC}}} \quad (2)$$

The terms are as follows: τ_B and τ_C are the base and collector transit times, I_C is the collector current, C_{je} is the emitter-base junction depletion capacitance, C_{BC} is the base-collector capacitance, and R_C and R_E are the emitter and collector resistances. Increasing R_B does not affect f_T, while the increased C_{BC} has a minor effect on f_T. However, both have a more pronounced effect on f_{MAX}.

A comparison of layouts A and B, using layer structure one, shows the effect of adding a small gap between the emitter and base metals. In both designs, the base contact was isolated, thus the only difference in the structures was due to the separation between the emitter and base metals. For geometry A, the separation between emitter and base metals was due to the semiconductor undercuts caused by wet etching. These undercuts were approximately 50 nm. The addition of a 0.15 μm spacer in geometry B increases the distance current must travel through the highly resistive base by a factor of 4. This separation is causes R_B increases from 35 ohms to 51 ohms.

In addition to increasing R_B, the realignment also increased the cross-sectional size of the base-collector junction. The larger area caused C_{BC} to increase from 19.9 fF to 22.9 fF. The increased parasitics have a slight effect on the f_T, as it decreases by 8%, but a much larger effect on f_{MAX}, as it decreases by 32%. Thus even a small gap between the base and emitter, has detrimental effects to the device parasitics.

The next comparison is between geometries A and C, using layer structures two and three. Geometry C also has a realigned base with a larger gap between the emitter and base than B. This causes R_B to increase from 64.3 ohms 107.8 ohms. Geometry C does not isolate the base contact and utilizes a realigned collector etch, resulting in an increase in C_{BC} from 30.4 fF to 78 fF. Additionally, increasing the number of fingers does not have a significant

effect as the parasitics scale with the number of fingers. The R_B did not change appreciably with the addition of four fingers and the C_{BC} per finger decreased to 54 fF/finger.

The comparison between the non-ideal geometries in B and C and the ideal geometry in A demonstrates the shortcomings of the current layout. Any gap between the emitter and the base will cause a substantial increase in R_B. The additional junction area will cause C_{BC} to increase, as well. A realigned base-collector etch and a non-isolated base contact layer causes additional increases in C_{BC}. The magnitude of the increase in R_B and C_{BC} from geometry A to C shows that the conventional power device layout is inadequate for the high speed, high power circuits.

Methods to change the layout such that the transistors will achieve high speed performance, allowing for multiple fingers, and are compatible with a sub-micron emitter size are as follows. The base metal should be self-aligned. The effects of even a small 0.15 μm gap seriously degrade performance. To allow the base metal to be self-aligned, a sidewall spacer or using undercuts must be implemented to avoid emitter-base shorts. Additionally, a self-aligned collector etch would decrease the C_{BC}. A third factor to consider is shrinking the emitter and base sizes also makes the size of the base contact more of a factor than the current device. Implantation or undercuts might serve to isolate the base contact. The implementation of these techniques would allow devices to enter the high speed, high power regime.

4. Conclusion

Transistors have been fabricated using three different geometries to determine the effects that realigned base metal has on device parasitics, then compares a popular power transistor geometry with a design made for the purpose of reducing parasitics. The realigned base causes a 42% increase in R_B and a 15% increase in C_{BC}. Comparing the power geometry with the high-speed geometry, there is an increase in C_{BC} by over 100% and 68% in R_B. The drastically increased parasitics demonstrates why the current power structure needs to be modified for use in high speed, high power applications.

Intelleip for supplying structures 2 and 3, and Dr. Richard Chan and Dr. David Caruth for their valued technical discussions.

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ACRONYMS:

f_T: Cutoff frequency
BV_{CEO}: Breakdown Voltage, Collector-Emitter, With Base Open
HBT: Heterojunction Bipolar Transistor
SHBT: Single Heterojunction Bipolar Transistor
DHBT: Double Heterojunction Bipolar Transistor
PHBT: Pseudomorphic Heterojunction Bipolar Transistor
SI: Semi-Insulating