Process Considerations for Manufacturing 50 μm Thinned III-V Wafers

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ABSTRACT:

Device performance requirements for heat dissipation continue to drive products to thinner substrate thickness. However, processing of wafers thinned to 50μm creates new challenges for handling these fragile substrates. Breakage of substrates during manufacturing can create significant expense and the risk of damage is increased as the number of steps for backside processing increases.

TriQuint Semiconductor has successfully developed and demonstrated a process for manufacturing devices on 50μm thinned III-V substrates. This paper focuses on the process controls and considerations needed to manufacture devices on thinned substrates. Process considerations at several points in the thin wafer flow (including wafer mounting, backside metallization, demounting and die singulation) will be discussed.

WAFER MOUNT:

Due to the intrinsic brittleness of III-V compound semiconductor materials, wafers must be temporarily bonded to a rigid carrier while being processed through backgrind, photolithography, metallization and substrate via etch steps during backside processing. Bonding can be achieved by various methods, such as thermal or UV release film, wax or UV cured optical adhesive. With all of these bonding methods, additional precautions must be taken to ensure that the device side of the wafer is protected from both chemical and mechanical damage.

TriQuint Semiconductor utilizes a UV curable optical adhesive and protective negative resist coating to bond wafers to a sapphire carrier substrate. The negative resist coating must be of sufficient thickness to completely cover all frontside topography so that the optical adhesive layer does not contact any of the frontside metallization. Debonding is achieved by dissolving the negative resist layer since, once cured; the optical adhesive becomes virtually insoluble in solvents commonly used in semiconductor device processing. We have found that the cured optical adhesive is required to keep the thinned wafers bonded to the supporting sapphire carrier during the substrate via plasma processing.

BACKSIDE METALLIZATION:

Wafers thinned to 100μm, 50μm or less become increasingly susceptible to the stress effects of applied thin films. The stress of epitaxial films can cause significant bowing of III-V wafers after the carrier substrate has been debonded from the wafer. If not accounted and compensated for, this stress can lead to yield loss due to wafer breakage during the wafer debonding process or parametric yield loss due to poor thermal contact during electrical probe.

Following substrate via formation, TriQuint Semiconductor sputters a coating of TiW/Ni/Au that acts as the seedmetal for the gold plating on the backside of the device. The stress in this layer is adjusted to compensate for curvature of the wafer induced by the epitaxial layers. This adjustment is made by varying the deposition pressure as seen in Figure 1. By careful tuning of the stress in the seedmetal layer, the curvature of the thinned wafer is minimized.

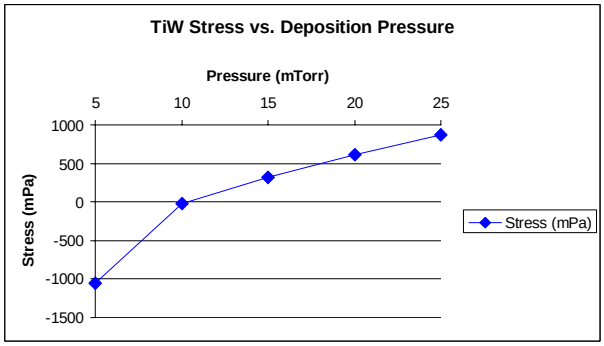

Figure 1
TiW film stress as a function of deposition pressure

WAFER DEMOUNT:

As indicated by the terminology of "temporary bonding", wafers must be removed from the carrier substrate at the conclusion of backside processing. This demount step can be the source of significant wafer breakage with 50μm thinned substrates. The demount step must completely debond the wafers from the carrier substrate with no residue remaining on the wafer. TriQuint Semiconductor has developed a demount process that consists of a multi-step chemical process that debonds the wafer from substrate and also removes the protective resist layer at the same time.

As with any chemical process, the first consideration must be to select chemicals that are compatible with the substrate wafer used, the materials deposited during the device fabrication process and that can be safely implemented into the fabrication environment. Secondly, the process developed must be robust and minimize cycle time. TriQuint Semiconductor has developed a debonding process that utilizes chemicals commonly found in semiconductor processing. These chemicals are used to dissolve the sacrificial negative resist layer applied to the wafers prior to bonding them to the supporting sapphire using the optical adhesive. As stated previously, the optical adhesive is not normally soluble in these chemicals and remains on the sapphire supports which must be cleaned in a separate cleaning process.

When developing the debonding process for 50µm thinned wafers, it became apparent that the turbulence generated by normal processing in overflow weir tanks was causing wafers to crack and break during the process. Attempts to adjust the turbulence by adjusting flow rates failed to improve the debonding results. We found that baffling the incoming flow resulted in a substantial improvement to the debonding process (Figure 2).

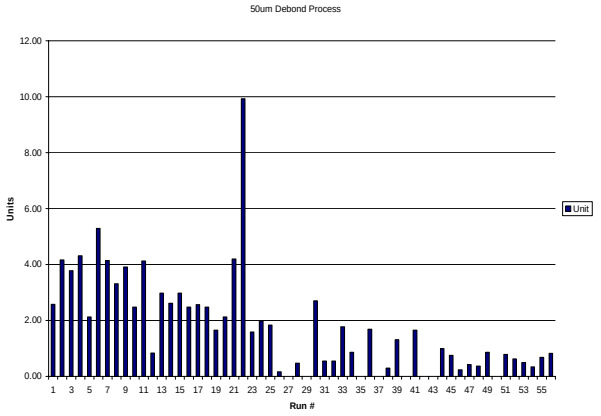

Figure 2

<u>DIE SINGULATION:</u>

Die singulation may be achieved by utilizing either wafer scribe and break methods or sawing. TriQuint Semiconductor utilizes both methods for die singulation for 50µm thinned wafers. This paper will focus on the process considerations for sawing 50µm thinned wafers. Tape selection for the saw process was determined to be the yield limiting characteristic in achieving high yields at die pick on 50µm thinned III-V substrates. Greater than 97% die yield from pick has been achieved with excellent quality after optimization of the tape selection and die pick process.

In developing a saw process for 50µm thinned wafers it is important to consider the physical nature of the process in terms of force from the saw blade moving through the material, the depth of the cut into the supporting tape and the cooling water being accelerated across the wafer by the blade. Tape must be selected so that die are held securely during the singulation process but can be easily removed during the die pick process after singulation. Designed experiments were conducted focusing on tapes from various vendors (Table 1) to optimize the die singulation process.

Table 1:

Tape Designation	Adhesive Thickness (µm)	Adhesion after cure
A	15	14g/25mm
B	10	3g/25mm
C	5	0.1g/20mm

One experimental layout and the results of the test are found in Table 2. The figure of merit used in this experiment was the percentage of die exhibiting defects after die pick. The best results were obtained using tape C which has the thinnest adhesive layer and lowest adhesion after cure.

Table 2:

StdOrder	RunOrder	CenterPt	Blocks	UV Expose	Saw blade	Post Clean	UV Tape	Bad Die%
3	1	1	1	Low	down	N	A	0.0
4	2	1	1	High	down	N	C	3.4
5	3	1	1	Low	up	Y	A	5.2
7	4	1	1	Low	down	Y	C	0.0
1	5	1	1	Low	up	Y	C	0.0
8	6	1	1	High	down	N	A	5.7
6	7	1	1	High	up	N	C	0.0
2	8	1	1	High	up	Y	A	4.9
9	9	1	1	High	down	Y	A	20.0
10	10	1	1	High	down	Y	A	19.0
12	12	1	1	High	down	Y	A	32.0

These results support a theory that during the saw process the adhesive is pushed up into the substrate via and is subsequently protected from the UV exposure to reduce the tack level of the adhesive. When attempts are made to remove the die at the pick process this high tack area causes a plug of adhesive to be left in the substrate via. The reduction in adhesive thickness minimizes the amount of high tack material on the interior of the substrate via and allows for die to be removed without residual material.

CONCLUSIONS

Developing processes for III-V semiconductor wafers thinned to 50μm and beyond poses an entirely new realm of difficulties as thin film effects begin to dominate the intrinsic strength of the substrate material. Special considerations must be taken with regards to stress management of deposited films and to the stress induced by the chemical and mechanical processing that must be done to produce the final devices. As device performance requirements continue to drive substrate thickness to progressively smaller sizes, new process development will follow to allow for manufacturability of those devices.

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ACRONYMS

UV: ultraviolet