Carrier techniques for thin wafer processing

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Abstract

Three different types of carrier techniques have been investigated and developed: thermal release tapes, solvable thermoplastic glue layer and mobile electrostatic carrier. These carriers were applied for manufacture of ultra-thin RFID chips, 12 µm thin CMOS image sensors and to a new process sequence that enables the formation of solder balls at the front side of an already thinned device wafer. Technical capabilities of different carrier techniques are compared with respect to allowed temperature range, type of bonding and de-bonding mechanism and their compatibility with typical wafer fab processes. Mobile electrostatic carriers were used to perform solder ball bumping at 55 µm thin silicon wafers. The process sequence demonstrates the capability of electrostatic carrier technology to enable thin wafer processing at elevated temperatures.

INTRODUCTION

The increasing demand for thin semiconductor devices have required more and more sophisticated solutions for their manufacturing processes. Appropriate support systems are a basic need for secure handling and processing of very thin semiconductor device wafers. Generally this is accomplished by temporarily bonding a rigid carrier substrate onto the front side of a device wafer before thinning. Well known techniques use polymeric bonding agents like wax, solvable glues or thermally releasable adhesive tapes [1]. Further manufacture concepts are based on bonding materials that can be released after UV laser irradiation through a transparent glass carrier [2]. Application of polymer based bonding techniques is limited to the temperature range below 200 °C. Further increased temperature stability is required in order to allow process steps like sintering of backside metal or plasma etching of dielectric layers. In contrary to adhesive bonding electrostatic attraction has the potential to enable thin wafer processing at elevated temperatures [3]. Recent development work at the authors' institute has lead to a new type of mobile electrostatic carriers based on silicon wafer substrates which were successfully applied to process steps like photo-lithography and plasma etching [4].

Next sections will describe following different types of carrier techniques: thermal release tapes, thermoplastic glue layers and mobile electrostatic carriers.

THERMAL RELEASE TAPES

Application of thermal release tapes has become a wide spread method in order to support wafers with low topographies during thinning processes. A carrier is attached to the process wafer by means of a double-sided adhesive tape with one side thermal releasable. Subsequently, backside grinding and etching down to 10µm can be performed. Removal of the carrier is performed by a heating treatment between 90 and 150°C. This method was also applied for wafers with high surface topography. In this case, device topography was embedded by an additional tape. Furthermore this method can be combined with the Dicing-by-Thinning technology (DbyT) as illustrated in Fig. 1. Dicing grooves are prepared at wafer front side with the trench depth corresponding to the projected chip thickness. Preparation of these chip grooves can be accomplished by means of a wafer saw or by silicon dry etching. After mounting the trenched device wafer to the carrier substrate the wafer pair is thinned from its backside until the chip grooves are opened.

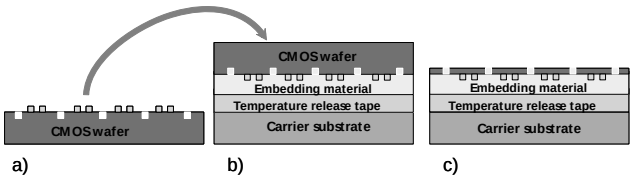

Fig. 1: Dicing-by-Thinning process for wafers with high topographies: a) Pre-patterning of scribe lines, b) Embedding of topographies and reversible bonding to carrier substrate, c) Result after thinning process.

Problems may arise when chemicals (etchants or polishing slurries) get in contact with the embedding material through the separation grooves. In order to overcome these difficulties we introduced a protective layer which is spun onto the wafer surface before taping. After wafer thinning the carrier substrate is lifted off by initiating the thermal release function of the thermal tape. Subsequently, all separated chips yet attached to the embedding tape were transferred onto a film frame carrier (see Fig. 2). The protective coating was removed after delaminating the embedding tape. Wafer thinning, chip separation and transfer was successfully conducted with 25 µm thin and flexible RFID chips for smart label applications [5].

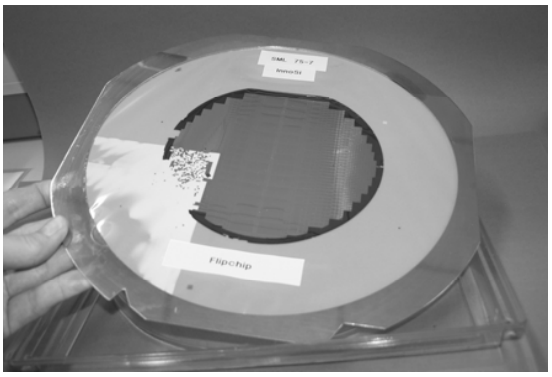

Fig. 2: Film frame carrier with 30 µm thin chips on thermal release pick-up tape; single chips were removed on the left side.

SOLVABLE THERMOPLASTIC GLUE LAYER

As second method for reversible bonding technique by means of polymeric materials we investigated thermoplastic glue layers which can be applied by spin-coating process. Using this method allows for very thin and uniform adhesive layers. This is of utmost importance when wafers of a final thickness in the range of 10 µm are to be prepared. Thickness variations in the adhesive film would directly result in a non uniform wafer thickness which is in most cases not tolerable. There's a second benefit when using such glue layers: the capability to embed surface topography. Especially when combining "Dicing-by-Thinning" technology with a final CMP polishing process performed at 20 to 10 µm thin device wafers we succeeded in best thinning results. The thermoplastic glue fills the front side chip trenches to a large extent and thereby prevents chip cracking during final CMP step. Fig. 3 shows a cross section of a 12 µm thin wafer processed according to DbyT-concept. Chips are already separated and are still attached to a carrier wafer by thermoplastic adhesive.

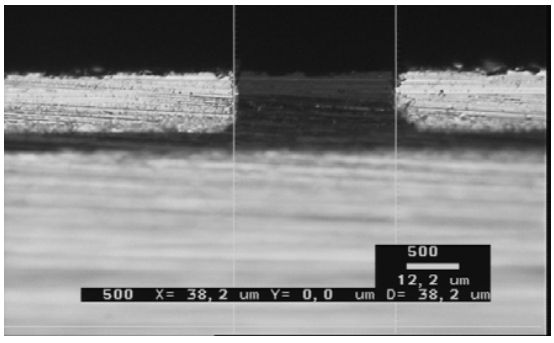

Fig. 3: Cross section of thinned wafer, mounted on a carrier substrate by means of a thin solvable glue layer.

In order to remove all thin dies the carrier wafer is immersed into a solvent bath and the glue is dissolved. All dies are released without any mechanical force and can be fished out of the bath. The process flow was applied to silicon CMOS image sensor wafers (diameter 200 mm). 10 – 15 µm thin sensor chips were prepared and their electrical functionality was proven [6].

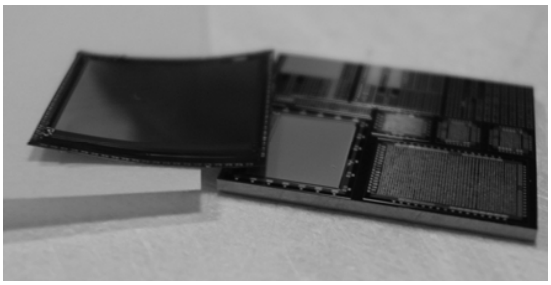

Fig. 4: 12 µm thin CMOS image sensor placed on a sheet of paper (left) and compared to a chip of standard thickness (right).

MOBILE ELECTROSTATIC CARRIERS

Electrostatic forces offer the unique opportunity to realize a reversible bonding technique without using polymeric bonding materials. Therefore bonding and de-bonding of thin wafers onto electrostatic carriers can be achieved within very short time, in a repeatable manner and without any constraints regarding surface contaminants from bonding agents. Fig. 5 shows an example of a mobile electrostatic carrier prepared on a silicon wafer substrate and the adjacent charging unit which provides 200 V DC voltage to initiate the electrostatic fixation [7].

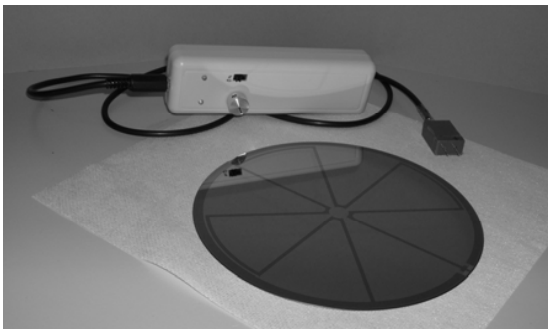

Fig. 5: Mobile electrostatic carrier made on silicon wafer substrate and hand-held power supply.

Most important feature of this carrier technique is its ability to maintain electrostatic attraction after disconnection of power supply for a long period of time. It was already shown that permanent polarization state remains active at temperatures even above 400 °C [3]. Fig. 6 shows the voltage decay at the contact pads of a mobile electrostatic carrier, measured at room temperature and with a thin wafer attached onto the carrier. Room temperature stability of the charging status keeps constant for many days and thereby offers a new and easy technical solution for transport, storage and handling of thin and fragile wafers. The long duration time of the polarized state of the carrier is also

confirmed by fitting experimental data with an exponential decay curve. Fit results indicate an impressively high portion of constant polarization, which is around 160 V when initial charging was performed at 200 V (see Fig. 6).

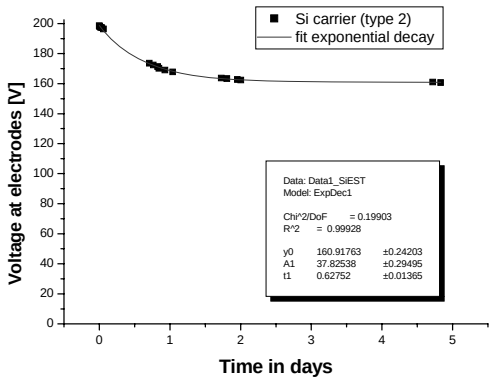

Fig. 6: Electrostatic potential measured at a mobile electrostatic carrier after removal of charging unit performed at 23 °C.

Electrostatic carriers have been prepared on ceramic, glass and silicon wafer substrates [4]. For applications in GaAs technology also sapphire substrates would be very desirable in order to match coefficients of thermal expansion of carrier and device wafer.

BUMPING OF THIN WAFERS BY MEANS OF MOBILE ELECTROSTATIC CARRIERS

Solder bumps are widely used for flip chip assemblies and chip scale package (CSP) technologies. However, thinning of wafers with solder balls having a diameter of 100 – 250 µm is a challenging task. Actually wafer thickness below 250 µm couldn't be reached by backside grinding due to high risk for wafer breakage. Mobile electrostatic carriers now offer the possibility for a new process sequence: After deposition of the under bump metallisation (UBM; e. g. Ni / Au, 2 – 5 µm in thickness) the wafer is first thinned by standard backgrinding process. The ground wafer may then be attached onto a mobile electrostatic carrier and undergoes further stress-relief processes like spin-etching or dry etching. Afterwards the thin wafer is transferred onto another electrostatic carrier and subsequently is introduced into the bumping sequence. This comprises solder paste deposition by stencil printing and solder reflow in a belt furnace at temperatures around 250 °C. Fig. 7 shows a 55 µm thin test wafer, diameter 150 mm, attached onto a mobile electrostatic carrier. Solder balls are already formed and are visible along the chip layout. After bumping wafers were removed from the carrier and diced by a conventional wafer saw. Final SEM inspection, see Fig. 8, shows the amazing relation between chip thickness and solder ball dimensions.

It should be mentioned that grinding of wafer having solder balls of 140 µm in diameter on top would definitely result in broken wafer substrate. Therefore bumping of a thin wafer is suggested instead of thinning a bumped wafer [8]. According to this new concept no restriction in wafer thickness and or wafer diameter does appear.

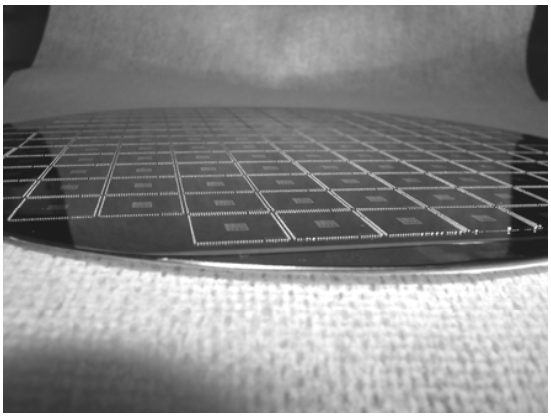

Fig. 7: 55 µm thin test wafer fixed onto a mobile electrostatic carrier.

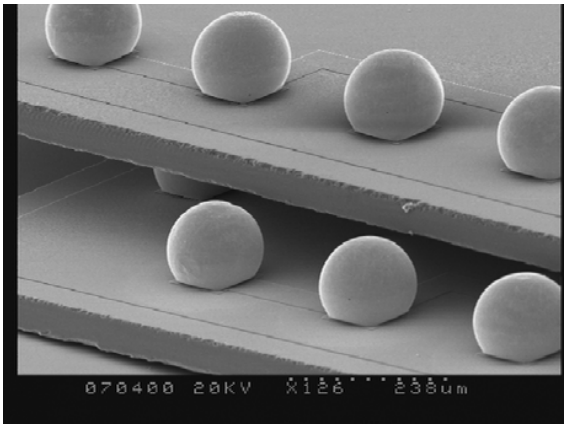

Fig. 8: SEM picture of 55 µm thin single chips; solder ball bumping was performed after thinning.

COMPARISON OF CARRIER TECHNIQUES

Thermal release tapes are easy to apply and enable manufacture and handling of 20 – 100 µm thin, flexible wafers and dies. Difficulties have been found when CMP polishing in combination with Dicing-by-Thinning concepts should be realized for chip thickness below 20 µm. Due to low thermal resistance of polymer tapes the possibility to run processes at the backside of thinned wafers is strongly limited. Furthermore tapes cannot seal the wafer edge during "under water" processes. Penetration of process liquids like water and solvents often leads to delamination of the tape close to wafer edge.

Thin thermoplastic glue layers allow for highly uniform wafer thickness, also in combination with CMP polishing and DbyT techniques. Temporary adhesive bonding by thin glue layers also enable low temperature backside processes like photolithography and metal sputtering. However, dissolving of glue layers and removal of residues require further technical efforts.

Mobile electrostatic carriers open the door for high temperature backside processing of thin wafers. Technical limitations occur with processes in liquid environments due to penetration of fluids between carrier and device wafer. In principle this risk might be reduced or stopped by applying a soft seal ring or layer on top of the electrostatic carrier. However, this would then reduce thermal stability.

TABLE 1
COMPARISON OF REVERSIBLE BONDING TECHNIQUES

	Thermal release tapes	**Thermoplastic adhesive**	**Mobile electrostatic carrier**
Application of Bond layer	Tape lamination	Spin-coating	none
Thickness of bond layer	100 – 300 µm	1 – 5 µm	none
Temperature stability	80 – 130 °C	ca. 150 °C	> 400 °C
Process capabilites	Wafer grinding, spin-etching,	grinding, etching, polishing, sputtering, lithography	Dry etching, layer deposition, lithography, sintering, …
Debonding mechanism	Heat induced	Dissolve chemically	Electrical discharge
Necessity for cleaning	In some cases	yes	no
Possible product applications	Thin, flexible semiconductors	3d-integration, ultra-thin devices	Power-, discrete-, solar cell-, GaAs-, opto-electronic devices

With respect to this short discussion it is concluded that there's yet not a single carrier solution that fulfills all requirements of thin wafer technology. As consequence this leads to a new task: development of appropriate wafer transfer concepts which allow a combination of different carrier techniques.

THIN WAFER TRANSFER

Because of the simple bonding and de-bonding mechanism mobile electrostatic carriers are specifically qualified for transfer processes of very thin wafers. Fig. 9 shows an example how to transfer a thinned wafer from a carrier with thermal release tape onto an electrostatic carrier.

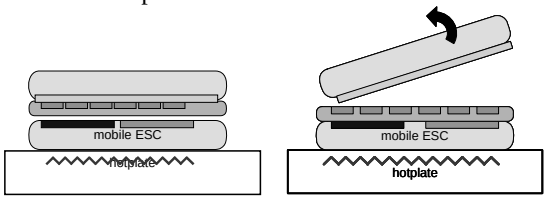

Fig. 9: Transfer of a thinned wafer from an adhesive tape based carrier (left on top) onto an electrostatic carrier (right side at bottom).

First the backside of the thinned wafer is put onto the electrostatic carrier. Charging the e-carrier leads to a triple wafer stack. By heating the underlying vacuum hot-plate the adhesion of the thermal release tape gets lost and the first carrier on top of the stack can easily be removed. The thin wafer itself is always connected to a rigid carrier. This transfer concept was used successfully for the demonstration of solder ball bumping after wafer thinning. In this case wafer backside was attached onto the electrostatic carrier, subsequent front side processes could be performed straight forward.

Of course it will be also possible to first transfer a thinned device wafer onto a standard porous vacuum chuck and then attach the surface of this device wafer onto an electrostatic carrier. Such handling sequence enables further backside process steps for thin wafers attached onto a mobile electrostatic carrier.

CONCLUSIONS

Temporary bonding techniques enable secure handling and processing of very thin and fragile semiconductor substrates. Ultra-thin silicon devices were prepared by means of reversible adhesive tapes and solvable glue layers. Electrostatic carrier open the door to high temperature processing of temporarily attached thin wafers. In order to demonstrate the applicability of mobile e-carriers a bumping process for 55 µm thin silicon wafers could be realized successfully.

It is supposed that appropriate selection of carrier techniques for specific process steps will lead to new manufacture concepts for very thin and fragile semiconductor substrates in the near future.

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