

# THE ROLE OF SUBSTRATE DISLOCATIONS IN CAUSING INFANT FAILURES IN HIGH COMPLEXITY InGaP/GaAs HBT ICs

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## Abstract

**A novel MSI circuit and reliability test method has been developed to measure the probability of infant failure in InGaP/GaAs HBTs. This circuit enables simultaneous reliability testing of 200 HBTs per circuit, and has been used routinely to test 12,800 HBTs/wafer (and sometimes 100, 000HBTs/wafer) to measure the probability of infant failure Pqf on each wafer. We have applied this MSI reliability test method to more than 100 production HBT IC wafers and many experimental wafers. With these tests, we have identified a new HBT failure mode, for which a very small fraction of HBTs ( $P_{qf} = 10^{-3}$  to  $10^{-4}$ ) fail by beta degradation much sooner than the main HBT population. Moreover, the probability of infant failure Pqf is proportional to the substrate EPD, with a constant of proportionality approximately equal to the emitter area. This observation is consistent with a model where any HBT whose e-b junction is pierced by a substrate dislocation will suffer beta degradation much sooner than its companions. This data has motivated Agilent to procure substrates with the lowest possible EPD for the manufacture of high complexity HBT ICs with sufficient reliability for use in Agilent instrument products.**

## INTRODUCTION

As the transistor count in HBT IC technology increases, it becomes increasingly important to determine the incidence of early or "infant" failures (i.e., the probability of and rate in time of HBT failures for any early failure mode(s)). This is necessary to insure that the reliability of complex HBT ICs is acceptable, and to assess the need for burn-in screens or other such methods to reduce infant circuit failure rates to acceptable levels. For example, if the probability of infant failure ( $P_{qf}$ ) for an individual HBT during the product lifetime is  $10^{-4}$ , then a simple amplifier circuit with 8 transistors should have probability of infant circuit failure of 0.08%. This failure probability is small enough to ignore in most practical applications. On the other hand, for a circuit

with 500 transistors, this same  $P_{qf}$  for the individual HBT would predict probability of infant circuit failure of 5%. This probability of failure is unacceptably large in many applications. Unfortunately, typical high temperature operating life (HTOL) tests are done on relatively small samples of discrete HBTs (typically <100). While these tests give a good indication of the MTTF and sigma for the main HBT population in the process, the small sample sizes are inadequate to measure the probability of infant failure  $P_{qf}$  at the  $10^{-4}$  level, and this measurement of  $P_{qf}$  is required to support high complexity circuits (e.g., 500 HBT/ckt). Even assuming that process variations did not cause  $P_{qf}$  to vary appreciably from wafer to wafer (which is too optimistic), it would be very difficult to test enough HBTs using such discrete HBT tests to determine  $P_{qf}$ . For example, if 50 discrete HBTs were stressed per wafer on 400 wafers, the total sample size would still be only 20,000 HBTs. This is clearly too few HBTs to accurately measure  $P_{qf}$  at the  $10^{-4}$  level. To enable the measurement the probability of infant failure  $P_{qf}$  at this level, and to assist in the failure analysis in our HBT process, a dedicated and highly parallel MSI reliability test circuit and test methodology were developed.

## RELIABILITY CIRCUIT

The majority of HBT failures are associated with beta degradation so the MSI reliability test circuit was designed to detect that failure mode. This MSI circuit was first described by Yeats [1], and a schematic of the basic test cell is shown in Figure 1. The cell is repeated 50 times in a single array, and the array is repeated twice on a single chip measuring 1540x790  $\mu\text{m}$ . Thus, each chip has 200 Q1 HBTs which are all under stress. In this circuit, each normally on transistor (Q1) is paired with a normally off transistor (Q2); this is accomplished by biasing the Q2 transistor bases at a voltage more negative than the Q1 bases through the use of a Schottky diode and resistor  $R_d$ . When the beta degrades in the Q1, the increase in base current  $I_{b1}$  causes a decrease in base and emitter node voltages  $V_{b1}$  and  $V_{e1}$ , because of the additional  $I \cdot R$  drop across  $R_{bb}$ . The

high value of  $R_{bb}$  (5 kohm) causes appreciable switching to

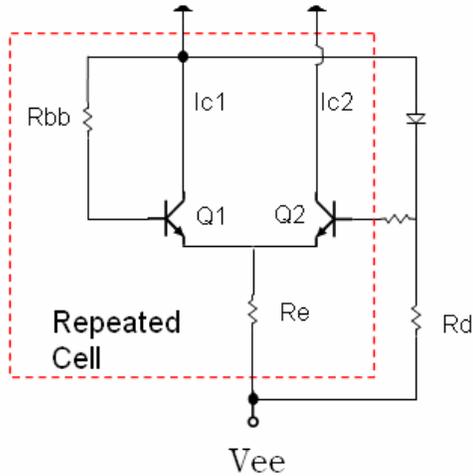


Figure 1. One cell of 100 cell MSI reliability test circuit

occur when beta of Q1 drops below about 30. If the Q1 emitter voltage drops low enough, it will turn on transistor Q2, which will then conduct  $\sim 1\text{mA}$  of  $I_{c2}$  current. Since the total  $I_{c2}$  is  $<1\mu\text{A}$  when there are no failed Q1's, it is easy to notice the  $\sim 1\text{mA}$  of  $I_{c2}$  generated by the beta failure of a single Q1 transistor. The  $I_{c2}$  line is shared by all the MSI cells, so if beta fails in any of the 200 Q1 transistors, it will cause detectable  $I_{c2}$  current to flow in the single  $I_{c2}$  sense line. In our implementation we have split up transistor Q1 into two smaller transistors to double the number of stressed transistors and thereby conserve circuit area. To enable stressing 100,000 transistors, about 12% of available 3-inch wafer area is required for MSI circuits.

#### RELIABILITY TEST

The bias and temperature stress condition used for the MSI circuit was  $J_c=0.6\text{mA}/\mu\text{m}^2$  and  $T_a=165\text{C}$  which gives a simulated junction temperature of  $T_j=230\text{C}$ . An HBT infant failure was defined as the appearance of sense current  $I_{c2}>1\mu\text{A}$  in the MSI circuit measured at  $T_a=20\text{C}$  after the stress. We initially stressed MSI circuits for 300-500 hours, but we found  $>50\%$  of the infant failures occurred in the first 100hrs, so the stress times were reduced to 168 hours, because the shorter stress time is adequate to detect most of the infant failures. The probability of infant failure (Pqf) was defined as the fraction of HBTs tested which failed in the MSI circuit after the 168hr stress. The observed values of Pqf were quite small ( $10^{-3}$  to  $10^{-5}$ ), so it was necessary to test large numbers of HBTs per wafer in order to accurately measure Pqf, especially for low EPD wafers which had the smallest Pqf. Sample sizes were adjusted so as to observe several infant HBT failures on each wafer to acquire adequate statistics; typically 12,800 HBTs/wafer were sufficient, but occasionally as many as 100,000 HBTs/wafer

were tested to observe an acceptable number of infant failures to determine Pqf.

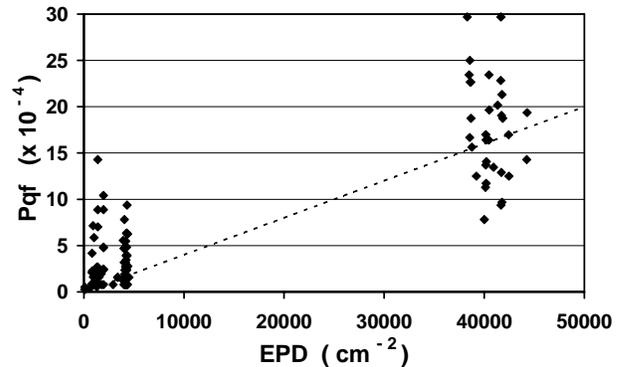


Figure 2. Measured Pqf vs substrate EPD level

#### RESULTS

Figure 2 shows the probability of infant failure Pqf value obtained from MSI circuit failures for many wafers plotted as a function of the etch pit density (EPD) of the substrate. The line drawn in Fig.2 is  $Pqf=A_{eb} \cdot EPD$  where  $A_{eb}=4\mu\text{m}^2$  is the area of the HBT emitters in the MSI circuit, and this gives a reasonable fit to the data. This fit of the data in Fig 2 suggests a model in which any HBT whose emitter-base junction is pierced by a threading dislocation from the substrate will fail by beta degradation much sooner than its dislocation-free companions

There are several sources of error which contribute to the scatter in the plot in Fig. 2, including sampling errors due to too few observed failures especially at low EPD. At higher EPD there is also significant scatter from uncertainty in the actual dislocation density, because of the difficulty of resolving the individual  $\sim 40\mu\text{m}$  etch pits at such high density (they tend to overlap). However, despite the scatter, there is a clear trend, and higher EPD substrates have larger probability of infant failure Pqf.

The lowest EPD data points in Fig. 2 correspond to three epi wafers grown on N+ VGF substrates provided by AXT. The N+ substrates can be grown with much lower EPD than semi-insulating substrates, and these had  $EPD \sim 100\text{cm}^{-2}$ . This EPD value is about 1/10 that of the very best semi-insulating VGF substrates which have  $EPD \sim 1000\text{cm}^{-2}$ . The measured Pqf for these N+ substrates was also about 1/10 that of the  $EPD \sim 1000\text{cm}^{-2}$  substrates. Specifically, for the N+ substrates, we observed 3 failed HBTs in 113,800 HBTs tested, which gives the extraordinarily low Pqf value of  $3E-5$ . While these ultra low EPD N+ substrates are not useful for our RF circuits, their very low Pqf value led us to an important conclusion. Dislocation driven beta failure is still the primary infant HBT failure mechanism in our process, even in the lowest available EPD semi-insulating GaAs substrates, and any further improvements in infant

failure Pqf will require still lower EPD substrates than are presently commercially available.

The Gummel I(V)s of HBTs which suffered infant failure were measured and compared with failed HBTs from standard HTOL tests. The infant HBTs were first identified by looking at failed MSI circuits under bias with an IR microscope to find which MSI cell(s) had switched state, as in the example shown in Fig. 3. The electroluminescence shows that stressed transistor Q1 in one cell turning off (dark), and the sense transistor Q2 is turning on (light), which indicates that beta in Q1 has failed. The failed cell was then pin probed to measure base and emitter voltages Vb1 and Ve1 on the failed Q1 while sweeping the MSI bias voltage Vee. From these Vb1 and Ve1 versus swept Vee, we constructed the Gummel I(V) for the infant and compared them with unfailed companions in the same MSI circuit. The infant HBTs had low beta (typically <15), but with Ic(Vbe) nearly unchanged from before the stress, and with a high base current Ib with a large n=2 component.

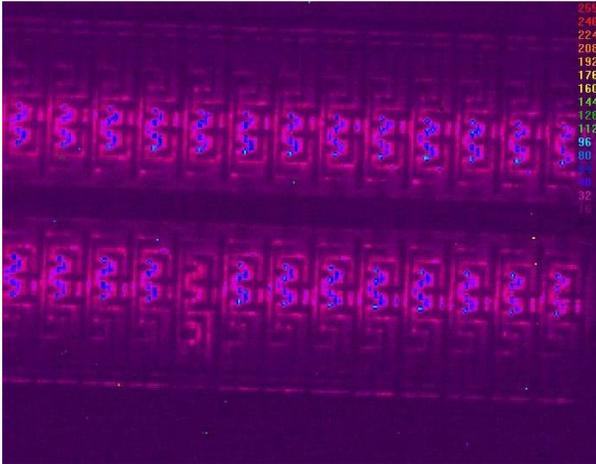


Figure 3. IR image of an MSI circuit with a switched cell indicating infant beta failure in a stressed HBT.

Despite the similarities in their Gummel I(V), the infant HBT failure mode differs in several respects from that of the conventional HTOL failures. First, at the chosen stress temperature ( $T_j=230^{\circ}\text{C}$ ) the MTTF for the infant failures is quite short (~50hrs) as compared with that of the main HBT population (estimated HTOL MTTF > 5000 hrs at  $T_j=230^{\circ}\text{C}$ ). The infant failure rate also has a much weaker temperature dependence than the main population ( $E_a = 0.42\text{--}0.58\text{ eV}$  for infants compared with 1.2eV for the HTOL failures of the main population (1)). By appropriate choice of the stress temperature, these differences between the infant failure mode and the HTOL failure mode enabled measurement of the very small infant failure probability Pqf without interference from beta failures caused by the tail of wearout distribution for the main HBT population (i.e., the

distribution typically characterized by MTTF and sigma from conventional HTOL tests [1,2]).

The infant failures also differ from HTOL failures, in that they exhibit a very gradual increase in Ib versus time. This fact was demonstrated using a variant of the MSI circuit whose operation is described elsewhere [3]. In this MSI circuit variant, unlike the standard MSI in Fig 1., the bias stress  $J_e$  on the stressed transistor Q1 can be held constant even as the beta degrades in that HBT. After an MSI failure was detected by high Ic2, this MSI was imaged under the IR camera to identify the failing HBT. This HBT was then repeatedly stressed at fixed  $J_e$  and elevated  $T_j$  and then re-measured for beta using special bias circuitry added to the MSI circuit. An example of the data is shown in Fig. 4, which shows the characteristically linear increase of Ib versus time for three failing infant HBTs under the noted constant stress conditions.

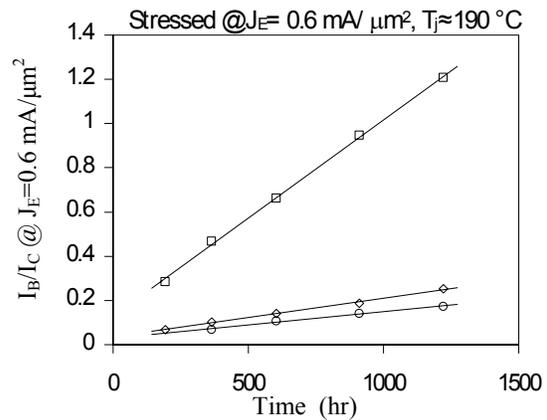


Figure 4. Linear increase in Ib with time.

This linear increase in Ib versus time at constant stress is quite different from the HTOL failures of the main HBT population which typically exhibit very abrupt increases in Ib when beta fails [1]. These differences between the infant and HTOL failure modes provide strong evidence that the infant failures are probably caused by a different mechanism from those of the main HBT population.

The gradual increase in Ib versus time for the infant failures also has an important practical implication for circuit reliability. It means that circuits which can still operate with very low beta (e.g., ECL logic ICs) will continue to function significantly longer under a given bias stress than circuits which are more beta sensitive like the MSI circuit. For example, ECL ring oscillators and a ring-oscillator driven divider which were used as reliability test vehicles exhibited more than 10X longer times to infant failure under the same bias and temperature stress as the MSI circuits. This behavior can be explained by the fact that these ECL circuits

stop functioning when  $\beta=2$ , which is about 1/10 the value needed for an MSI cell to switch ( $\beta=20$ ).

#### OBTAINING LOW EPD SUBSTRATES

The 3" semi-insulating GaAs substrates used in this work were obtained from various suppliers, but most were provided by AXT, Inc. and Freiberger Compound Materials. The dislocation density was measured by each supplier by etching sample substrates in molten KOH to decorate each dislocation with a pit, and then counting the etch pit density (EPD) at many sites and reporting the EPD as a wafer average. The high dislocation density substrates ( $EPD > 40,000 \text{ cm}^{-2}$ ) were all grown by Liquid Encapsulated Czochralski (LEC), primarily at Freiberger. The low dislocation density substrates ( $EPD < 6000 \text{ cm}^{-2}$ ) were all grown using the Vertical Gradient Freeze (VGF) technique. Both AXT and Freiberger provided the VGF substrates, and the lowest EPD substrates were grown by AXT. Significant efforts were made at both suppliers to produce 3" semi-insulating GaAs substrates by VGF with the lowest possible dislocation density and to accurately characterize the dislocation density by EPD measurements.

AXT performed many R&D growths in order to optimize the VGF growth conditions for low EPD, and they were very successful at repeatably producing boules with quite low EPD. This enabled Agilent to set an acceptance spec of  $EPD < 1200 \text{ cm}^{-2}$  to support HBT IC manufacturing. To achieve such a low EPD, AXT carefully controls several VGF growth parameters, the most important being:

- 1- Shape of melt/crystal interface
- 2- Crystallization velocity
- 3- Temperature gradient at the melt/crystal interface
- 4- Total temperature gradient

In this way AXT was able to reduce the EPD from  $\sim 2,500 \text{ cm}^{-2}$  to  $\leq 1000 \text{ cm}^{-2}$ . Further studies at AXT are continuing towards reduction of EPD levels to  $\leq 500 \text{ cm}^{-2}$ . These EPD values achieved at AXT are the lowest reported in the literature for semi-insulating GaAs substrates, and to our knowledge are the lowest EPD substrates commercially available.

#### CONCLUSIONS:

To our knowledge the present work is the first clear demonstration that substrate dislocations cause beta rapid failures in InGaP/GaAs HBTs, and that lower EPD substrates exhibit fewer infant failures. The failure mode associated with dislocations shows gradual beta degradation, in contrast to the abrupt beta failures seen in HTOL. These observations have motivated our intense collaborative effort with substrate suppliers to develop and obtain the lowest possible EPD semi-insulating GaAs substrates for HBT epi growth. Such low EPD substrates are essential to provide acceptable reliability for the high complexity InGaP/GaAs HBT ICs used in Agilent's instrument products. Clearly, as transistor counts in HBT ICs increase beyond 1000, even lower EPD substrates will be required for acceptable infant reliability of these ICs.

#### ACKNOWLEDGEMENTS

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#### ACRONYMS

EPD: Etch Pit Density  
HBT: Heterojunction Bipolar Transistor  
HTOL: High Temperature Operating Life  
MTTF: Mean Time to Failure  
MSI: Medium Scale Integration