On Wafer Reliability Test Bench for PHEMT and HBT Technologies

F. Bourgeois, M. Lanz, G. Jonsson, H. Stieglauer and D. Behammer

United Monolithic Semiconductors – GmbH, Wilhelm-Runge-Strasse 11, D-89081 Ulm – Germany
Phone: +49-731-505-3092, Fax: +49-731-505-3005, e-mail: bourgeoi@ums-ulm.de

Keywords: On Wafer Reliability, PHEMT, HBT, Life-test

Abstract

This work shows the benefits of testing the reliability on wafer directly after front-side process completion.

INTRODUCTION

Fast reliability testing is a key point for III-V technologies. This is particularly true when modifications have to be implemented on the production line. Such modifications can be sorted in four categories: raw material, new equipment, process step and design rule modifications. Endurance tests have to be performed to ensure that through the modified steps the reliability of the technology has not been changed.

High **T**emperature **O**perating **L**ife-tests (HTOL) is the common way of assessing the reliability of active devices like field-effect transistors, diodes or varactors. For III-V devices, these tests are usually done on packaged chips. The devices are completely processed including the full front-end and a complete backend process with wafer thinning, via-hole etching, dicing and packaging.

Knowing that in a standard process-flow the active devices are generally processed before the passive elements (inductor, resistor, capacitor) and before the backside, the time delay between the active devices' process completion and the reliability testing could take weeks.

A quicker reliability feedback can be obtained by testing the devices directly on wafer after the front-side completion. In the frame of this "time-to-answer" reduction, we have developed a **W**afer **L**evel **R**eliability (WLR) test system that is able to handle all the UMS technologies: MESFET, low-noise PHEMT, Power PHEMT and HBT. This system can stress devices at different temperatures (Tcase=25°C up to Tcase=200°C) for different bias points and perform the intermediate measurements without removing the wafer from the system. This allows a fast assessment of the electrical parameters' drifts and therefore a quick evaluation of the modification on reliability.

DEVICES AND TEST SETUP

The first type of **D**evices **U**nder **T**est (DUT) are PHEMTs (**P**seudomorphic **H**igh **E**lectron **M**obility **T**ransistors) from UMS low noise process PH25 with a gate length of 250nm and a gate width of 100µm. This technology is a single recessed, single side-doped AlGaAs/GaAs PHEMT structure. The gate is a dielectric assisted, aluminum based, T-shaped gate as shown in Figure 1.

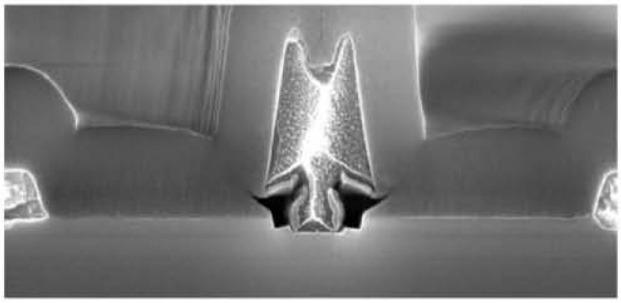

Figure 1. Cross-section of a PH25 device

The typical electrical performance of PH25 includes Idss (drain current at Vgs=0V) ~ 380mA/mm, pinch-off voltage Vg100 (Vgs at 1% of Idss) ~ -0.8V, maximum transconductance Gmax ~ 550 mS/mm (at Vds=2.5V), three-port breakdown-voltage Vbds ~ 7V and cut-off frequency Ft = 90GHz.

The second DUT type is a **H**eterojunction **B**ipolar **T**ransistor (HBT) from UMS power-HBT process HB20P as shown in Figure 2. This is a GaInP/GaAs HBT process especially dedicated to high power MMIC amplifiers for applications from C to Ku frequency bands. This process combines high power density (3.5W/mm) and high gain (14.5 dB at 10 GHz for a power cell of 8x40µm).

Figure 2. Cross-section of a HB20P device

The WLR setup has to fulfill two major requirements, in-situ HTOL and in-situ transistor parameters measurement.

A schematic description of our setup is presented in Figure 3.

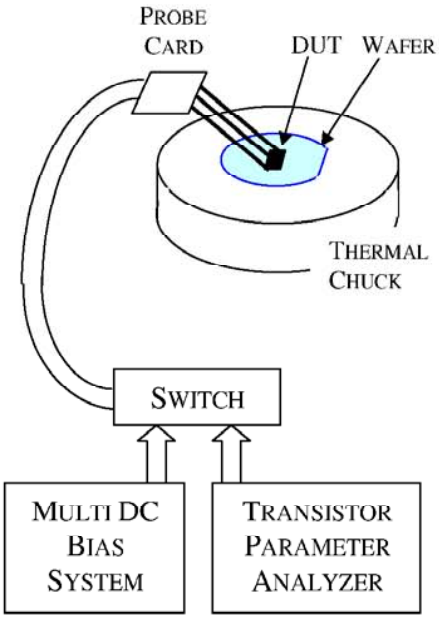

Figure 3. WLR system general schematic

The DUTs are contacted via a standard DC probe card with the appropriate decoupling network to avoid oscillations during the Life-test. This probe card is connected through a switch (Keithley 7705) to the multi DC biasing system (BILT: Modular DC bias system from iTest France) during the test or to the parameter analyzer (Keithley 4200) for the intermediate measurements.

This system has been developed to stress multiple parts simultaneously. In our configuration, the BILT system has 12 current/voltage [1] supplies allowing the test of 6 devices at a time: 3 devices per probe card. This system is scalable: the number of DUTs per wafer can be easily enhanced increasing the number of multi-bias systems and adapting the probe cards and the devices' layout on wafer. Figure 4 shows a schematic view on the pattern developed for the HBT technology. Figures 5 and 6 show examples of on-wafer intermediate measurements that can be performed by switching to the Keithley parameter analyzer at high or at room temperature.

Finally, it has to be noticed that this system does not replace a complete evaluation plan of a technology. We address here only the wearout mechanisms. Taking as hypothesis that for mature technologies the wearout mechanisms are well known, all the devices should degrade in the same way under the same stress conditions. This justifies the relative low amount of DUTs: we investigate the same degradation mechanism for all the parts.

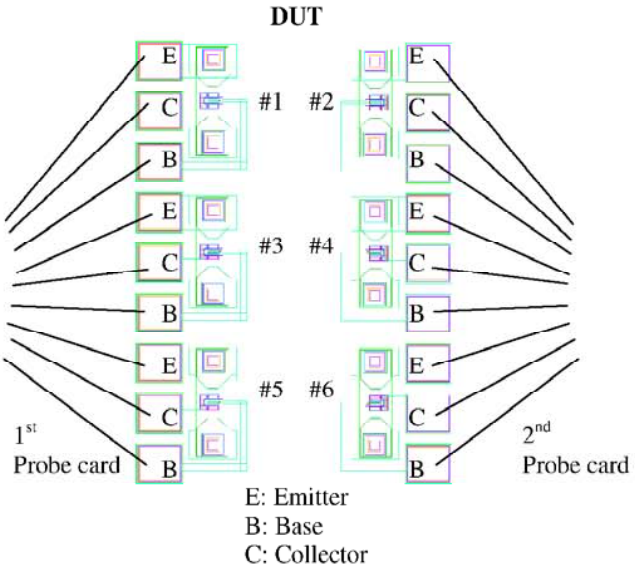

Figure 4. Schematic view of HBT pattern: 6 transistors with probe card connections.

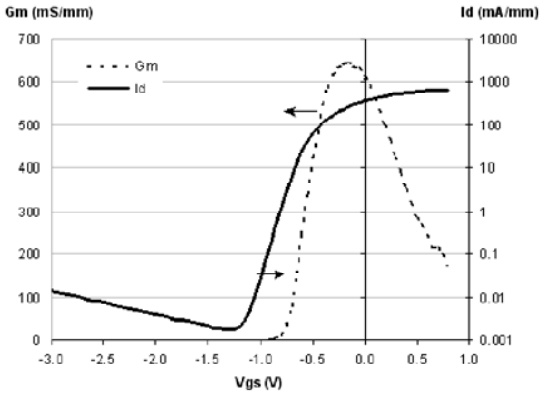

Figure 5. On wafer PHEMT transfer curve

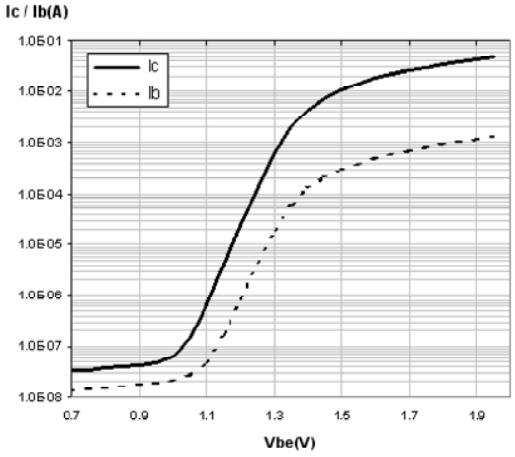

Figure 6. On wafer HBT Gummel plot

This WLR is only a verification test and does not replace a complete reliability evaluation. The other electrical tests defined in a qualification plan such as RF life-tests, DC test in humid environment and investigation of the useful-life degradation mechanisms shall be performed in a representative environment of the application (packaging, soldering, etc.).

THERMAL RESISTANCE MEASUREMENTS

Before starting the life-tests, a precise value of the thermal resistance of the DUT has to be known in order to calculate the junction temperature of the device. We used three types of electrical measurement to calculate the Rth of our PHEMTs and HBTs, each discussed below.

For the PHEMTs transistors, we used the measurement protocol from D. P. Estreich[2] and a pulse method. Estreich's method consists of using the gate of the transistor as "thermometer" measuring the metal's resistance variation with the temperature.

The second method used for the Rth calculation is based on pulse measurements. This method is also used to confirm the results obtained with Estreich's method.

The pulse method is illustrated in Figure 7. First, a DC measurement at room temperature of the direct characteristic Id = f(Vgs,Vds) is performed. The second step is pulsed measurements made at increasing case temperatures. The setup we use is a DiVa D225 pulse measurement system from ACCENT. The pulse duration is 100ns and pulse period is 1ms. This pulse-length and period minimize the effects of self-heating so that $T_{channel}$ is equal to T_{case}.

As shown in Figure 7, when the DC characteristic at room temperature and the pulse measurement at high temperature are superimposed in the saturation region, the junction temperature of the transistor is given by the case temperature of the pulse measurement. Table 1 compares the Rth calculated with both methods, Estreich's and pulse.

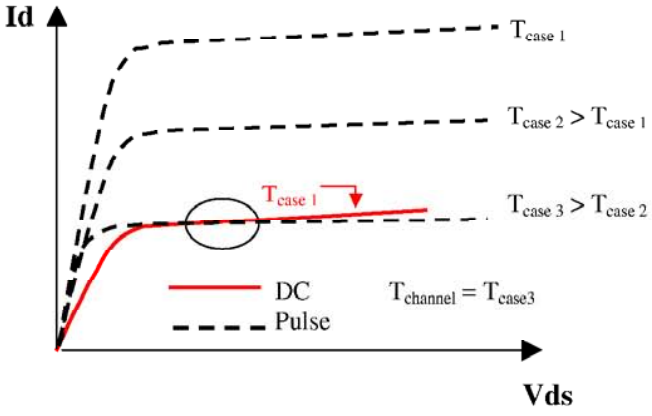

Figure 7. Pulse measurement method

TABLE 1
SUMMARY OF PHEMTS' RTH

Case Temperature (°C)	Estreich Rth (°C/W)	Pulse Rth (°C/W)
25	416	438
75	488	480
125	558	532
175	637	- *
225	708	- *

[a] To calculate the Rth at 175°C and 225°C, the pulse measurements should have been done up to 350°C, which is too high for the equipment.

For Rth calculation on HBT, we have used the well-established Marsh[3] method. Figure 8 shows the variation of the DC power with the temperature. For the transistor we use, a single finger HBT with an emitter surface of 2x30µm, the Rth is 750 °C/W.

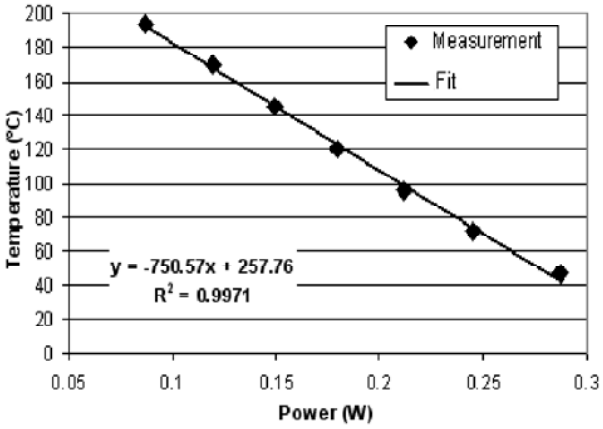

Figure 8. Rth of the HBT transistor

LIFE-TESTS RESULTS

In this section, we show the concrete application of this WLR test bench on a modification of the surface treatment of the PHEMT transistor and on the optimization of the passivation on the bipolar transistor.

Figure 9 shows the evolution of the gate current measured on a single finger transistor. The test conditions were Id=28mA, Vds=3.5V and a case temperature of 150°C. With the Rth values we have already calculated in the previous section, we achieve a junction temperature of 209°C. The DUT is a 100µm gate-width transistor.

Knowing that in our device the evolution of the gate current strongly correlates with the off-state breakdown voltage, we can predict a smaller degradation of this breakdown voltage with the surface treatment #1. Within a few hours we can distinguish between a suitable and a less

suitable treatment of the recess surface leading to a more reliable transistor.

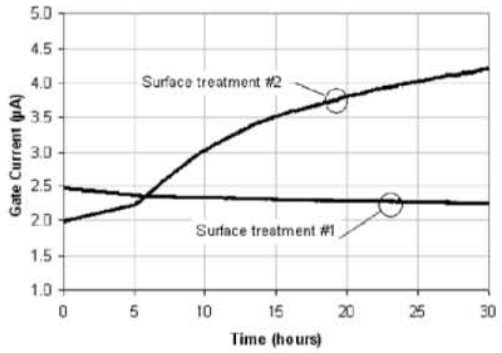

Figure 9. Evolution of the gate current on PHEMT transistor with different surface treatments

Figure 10 shows a similar test done on our HBT device. In this case, different surface preparations have been tested and the degradation of beta during the life-test has been monitored. The test conditions were Ic= 42mA, Vce=5.2V. Similarly, with the Rth calculated in the previous section, we achieve a junction temperature of 314°C with a case temperature of 150°C. In the same way as for the PHEMT transistor, within few hours we can distinguish between a suitable (Passivation #1) and a less suitable passivation (Passivation #2) of the HBT transistor.

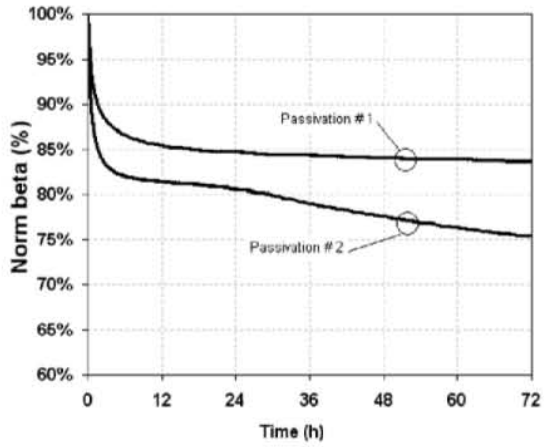

Figure 10. Evolution of the normalized beta of a HBT transistor with two different types of passivation

SAVINGS USING WLR

The last points we would like to discuss are the multiple advantages of making the tests directly on wafer.

The time saved for backside, back-end, mounting and initial measurement is around four weeks. Additionally, the active device or any other part can be tested directly without performing the complete front-end process, say 2 weeks. In total we're close to six weeks of time saved.

Another advantage is that this type of test does not involve all the company departments, but can be reduced to a small group of people: those responsible for the engineering and the reliability engineer. This way to proceed sets resources free that can be used to solve other problems.

Finally, the device under test can be really tested separately without the parasitic effects of other front-end, back-end and mounting steps: it is clear that the device reliability is tested and not the reliability of the mounting or wire-bonding process.

CONCLUSIONS

We have shown here the benefit of performing the reliability tests directly after wafer Front-End completion on two different technologies, a low noise PHEMT and a HBT. The major benefit is a drastic reduction of the "time-to-answer," helping the process engineer choose the more reliable process step. This approach also suppresses the parasitic effects due to back-end operations (soldering, bonding, packaging), and is useful during the development of new technologies like GaN to distinguish between the reliable and less reliable process steps very early during the development phase.

REFERENCES

[1] iTest, "BILT Facts" BILT General System Presentation.

[2] Donald. B. Estreich, **"A DC Technique for Determinig GaAs MESFET Thermal Resistance,"** IEEE Transaction on Components, Hybrids, and Manufacturing Technology, Vol. 12, No.4, Dec. 1989

[3] Steve P. Marsh, **"Direct Extraction Technique to Derive the Junction Temperature of HBT's Under High Self-Heating Bias Conditions,"** IEEE Transactions on Electron Devices, Vol. 47, No.2, Feb. 2000

ACRONYMS

WLR:	Wafer Level Reliability
HTOL:	High Temperature Operating Life-Test
DUT:	Device Under Test
HBT:	Heterojunction Bipolar Transistor
PHEMT:	Pseudomorphic High Electron Mobility Transistor