A Temperature Dependent Scalable Large Signal InP/InGaAs DHBT Model

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Abstract

A scalable large signal device model was developed for type-I InP/InGaAs/InP devices that is based on the UIUC SDD2 model. Through model segmentation and parasitic separation, the model is able to provide accurate modeling of high speed DHBT devices from 0.5 X 3.0 um^2 to 0.5 X 5.2 um^2 devices.

INTRODUCTION

Modern radio frequency and mixed signal circuit design has increasingly relied on compound semiconductor devices to push operating frequencies deep into millimeter-wave range. InP/InGaAs/InP heterojunction bipolar transistors are capable of achieving both a unity current gain frequency (f_T) and maximum frequency of oscillation (f_{MAX}) in excess of 300GHz as well as high linearity and good thermal performance, making them a prime technology for ultra-high speed and mixed signal circuit design [1,2]. Designing precision circuits with these devices has been problematic, however, due to the lack of accurate large signal DHBT device models. The industry standard VBIC model, for example, was developed for older silicon bipolar technology and does not completely model the physics of modern HBT devices. Effects stemming from the heterostructure nature of both junctions are poorly modeled in the VBIC model, which leads to poor large signal modeling of III-V devices. To design new higher speed circuits an accurate model is needed, one that is capable of modeling large signal nonlinear device characteristics.

Several models that are specifically based on modern HBT devices (AgilentHBT, HiCUM and UIUC SDD2) have been developed in an attempt to give a more accurate large signal modeling and more reliable circuit designs. The UIUC SDD2 (Symbolically Defined Device) model has been shown to be especially good at modeling large signal characteristics for both individual devices and complex circuits [3]. The SDD's strength is its ability to model carrier velocity modulation in the collector, current blocking of the base-collector junction, and self-induced thermal effects. The model however lacks emitter scalability and temperature dependence, limiting circuit designs to the use of only one size of device at one operating temperature.

A temperature dependent, scalable large signal DHBT model that is based on the UIUC SDD model is being developed and is the focus of this work. This new SDD2 model is currently capable of providing accurate DC, RF, and large signal modeling over emitter sizes from 0.5 X 3.0 um² to 0.5 X 5.2 um². The model, when compared with the VBIC model extracted and issued by the device manufacture, is shown to be far superior in modeling all aspects (DC, RF, and nonlinear large signal) of the device.

SCALABLE MODEL

The scalable SDD2 model is developed from the original UIUC SDD2 model, which at its foundation, is based on the Gummel-Poon integral charge control relationship derived for high current density bipolar devices [4]. The SDD2's model topology (figure 1) is developed for a standard mesa based heterojunction process. Working from the outside in, the model incorporates the parasitic capacitances and inductances of the short lengths transmission line contacts to the device that cannot be calibrated out, the extrinsic base-collector junction along with its associated capacitance, and extrinsic resistances and capacitances associated with the physical separation of these areas in a device layout. The parallel diodes, capacitor, and current source model the intrinsic device (the portion of the HBT directly beneath the emitter). It is here that the majority of the transistor action occurs.

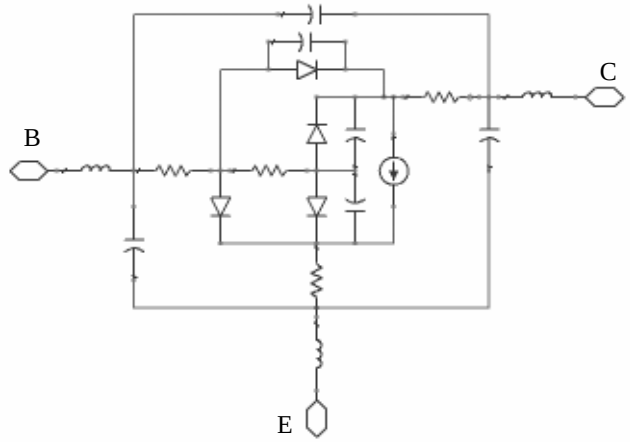

Figure 1: Scalable SDD2 Topology

This model, implemented as a Symbolically Defined Device in Agilent's Advanced Design System (ADS), is specifically based on the Vitesse VIP2 DHBT process. The scaling of the model is unique in that it closely models the physical scaling of modern DHBT devices. High-speed HBT devices (such as Vitesse VIP2) have been shrunk to such small sizes that the width of an emitter finger is often on the same scale, if not smaller than the minimum diameter of the via used to connect a metal layer to the semiconductor. To allow current flow into the device a via must connect the lowest metal layer and the emitter. Since in high performance device the emitter finger width is too small to receive a via, a fixed dimension emitter tab is added to the finger. This results in a separation of the emitter into a non-scalable region, the region around the emitter via where current is injected, and a scalable region, the remainder of the finger, (Fig 2).

The actual dimensions of the intrinsic device (the portion directly beneath the emitter) are quite different from the drawn length that is given to the circuit designer who is designing a circuit for this process. An attempt to model the scalable device parameters with only the given length and width would result in scaling errors, any fits that would be achieved would be non-physical. Decomposing the emitter into two separate regions in the SDD2 model, gives a much more accurate representation of device scaling than is achieved by simply scaling by the overall area of the device, and leads to the SDD2 model giving a much better model of the actual device performance than VBIC (Fig 3).

Effects from the emitter tab can be separated by first removing the finger modeling effects from the model and

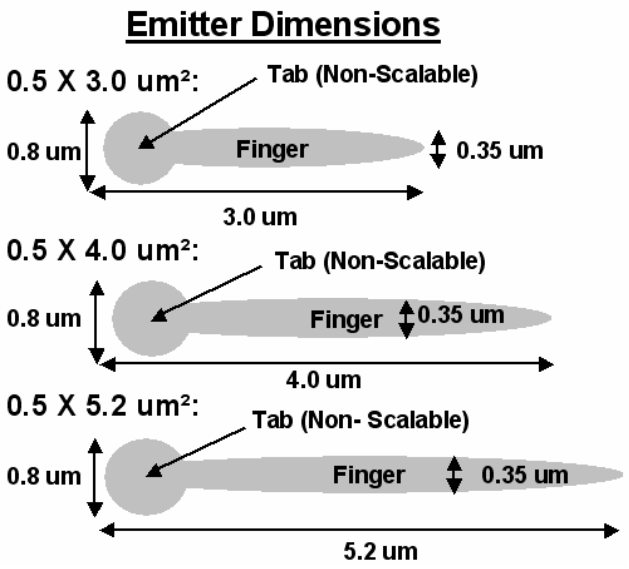

Figure 2: Realistic Dimension of High Speed DHBTs

modeling a device consisting solely of a tab (non-scalable emitter portion). After a model is developed for this simpler device, finger parameters can be added to the model and larger devices can be modeled. In this way, the individual contributions of the separate parts of the device can be determined separately, giving a fairly straightforward way of modeling the effects that result from the non-uniform current density across the emitter of the device.

In order to scale properly, each level of the model (intrinsic, extrinsic, and parasitic) must be scaled to reflect

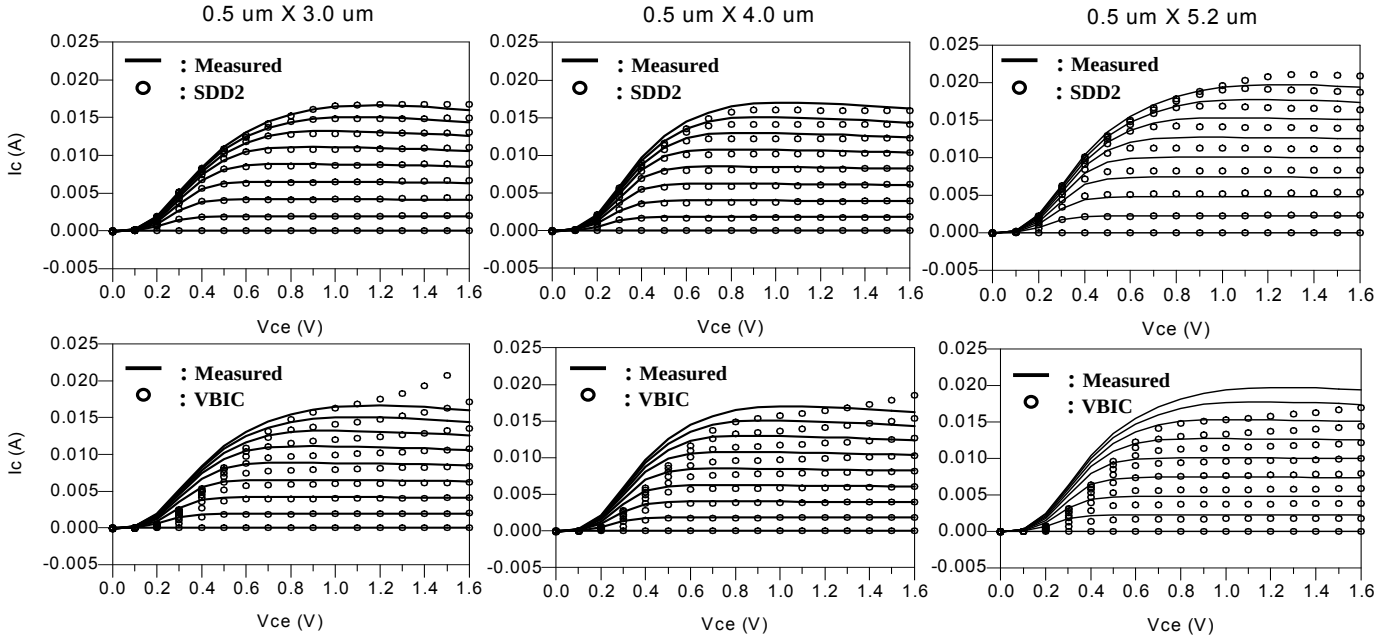

Figure 3: IV families of three measured Vitesse VIP2 DHBT devices of different size plotted with modeling results generated from both the Scalable SDD2 and VBIC model. (Vce: 0 – 1.6V, Ib: 0 – 160 uA)

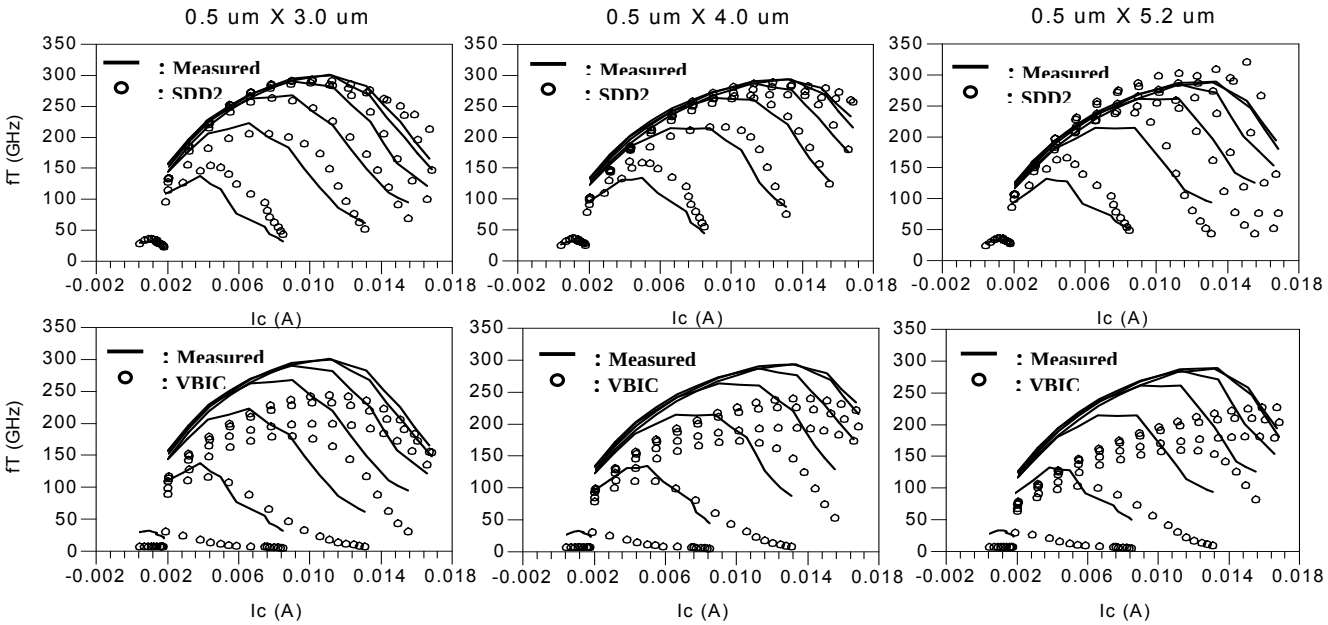

Figure 4: Measured f_T of three Vitesse VIP2 DHBT devices of different device sizes compared to results generated by Scalable SDD2 and VBIC model. (Vce: 0 – 1.4 V, Ib: 20uA – 160 uA)

the effect of dimension change on electrical properties. This is fairly straightforward for the intrinsic portion as resistances, capacitances, and currents of the emitter finger are either directly or indirectly proportional to the intrinsic finger size. However, there is not a direct relationship between the intrinsic size of the device and the electrical properties of the extrinsic and parasitic levels. Extrinsic parameters associated with the finger, such as the emitter resistance and extrinsic emitter base capacitance, are implemented as a function of finger area in a three term power series, while parasitic parameters are functions of the overall area.

VERIFICATION

Four means of verifying the scalable modeling ability of the SDD2 model are presented. Measured vs. modeled comparisons are shown for large signal DC current-voltage families, extrapolated f_T, forward gummel plots and large signal single tone measurements.

All DC measurements were taken using an HP4142B DC source monitor unit. Figure 3 shows the large signal DC modeling ability of both the scalable SDD2 and the VBIC (vertical bipolar inter company) model that was provided by Vitesse to use for circuit simulations. The scalable SDD2 model gives a much more accurate fit across all of the measured devices than the VBIC. The discrepancy between the models is most evident around the knee voltage and current where significant current blocking occurs. SDD2 also correctly models the drop in current at high biases caused by the self-heating effects of the device.

Forward Gummel measurements and model comparisons are shown in figure 5. The Scalable SDD2 provides nice fits to the measured data across all devices sizes.

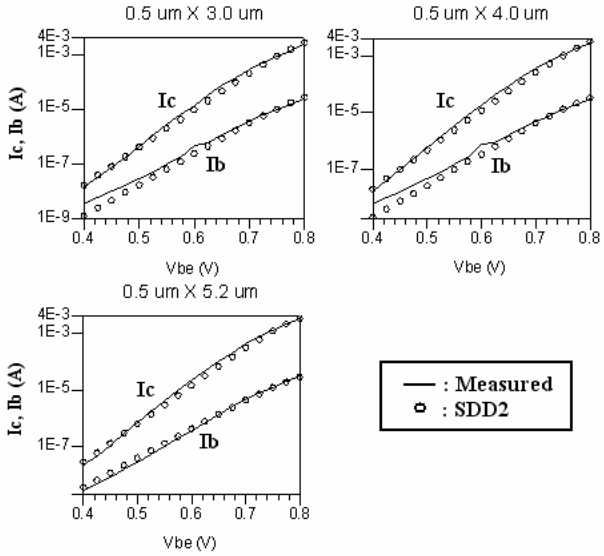

Figure 5: Measured and modeled forward Gummel data (Ic and Ib with respect to Vbe as Vcb is held at zero volts

The measured versus modeled unity current gain frequencies of the device (f_T) are plotted with respect to bias current and shown in figure 4 above. S-parameters of the devices were measured with an Agilent 8364A PNA and the fT at each bias was extrapolated with a -20 dB/decade slope from the calculated h_{21} at 40 GHz. The Scalable SDD2 model provides very accurate results, while the distributed VBIC model under-calculates the measured fT by approximately 50 GHz.

The ability of a model to accurately model the nonlinearity of a device is extremely important if it is going to be used to design any large signal circuit such as an

oscillator or power amplifier. One method of determining the linearity of a device is to send a large signal into the device and measure the power of the harmonics that are put out. This single tone measurement was carried out on the Vitesse devices using an Agilent 8364A PNA as a power source and an Agilent 8565E spectrum analyzer to measure the first 3 output tones (fundamental, 2nd and 3rd harmonic). This measurement was simulated in ADS through the use of a harmonic balance simulation, and modeled values for the output harmonics with respect to input power were obtained. Figure 6 shows the measured and Scalable SDD2 modeled values obtained for a 2 GHz input tone from –20 dBm to 0 dBm at a Vce = 0.6V, Ib = 140 uA bias.

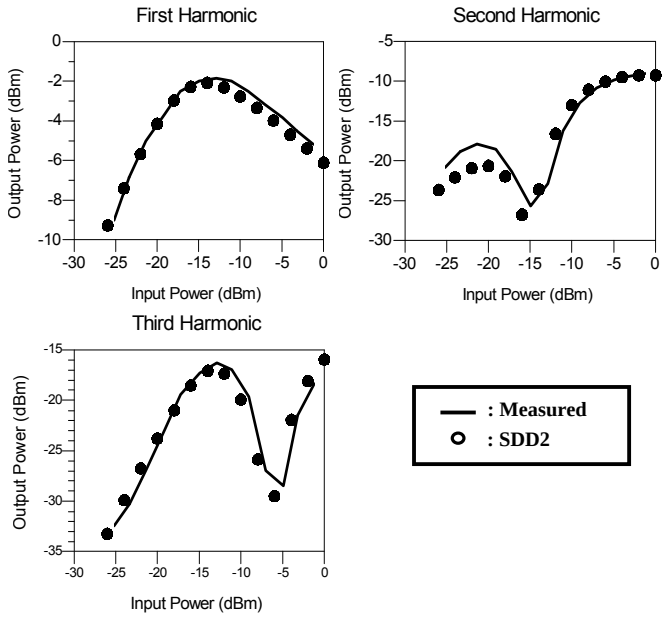

Figure 6: Measured and SDD2 modeled output of a 0.5 X 3.0 um^2 device with 2 GHz input tone swept from –25 dBm to 0 dBm

The SDD2 model gives a very nice fit at this high current bias point, which is in the highly nonlinear knee region of the device. The modeling of the fundamental output and third harmonic is extremely accurate across the entire power range. The second harmonic is under predicted at lower input powers, but converges with the higher power data. There is no VBIC modeled data given due the fact that the given VBIC model would not converge in simulation.

CONCLUSION

This paper describes the new Scalable SDD2 type-I DHBT model specifically created for InP/InGaAs devices. Through separating the device into a scalable and non-scalable portion, accurate DC, RF, and large signal nonlinear modeling results have been achieved for Vitesse VIP2 process DHBTs from 0.5 X 3.0 um^2 to 0.5 X 5.2 um^2.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
f_T: Unity Current Gain Frequency
f_{MAX}: Maximum Frequency of Oscillation
h_{21}: Two-Port Current Gain