HfO_2-based Metal-Oxide-Semiconductor Capacitors on n-InGaAs Substrate with a Thin Germanium Passivation Layer

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Keywords: InGaAs, GaAs, MOSCAP, HfO_2, Passivation, Capacitance, Ge

Abstract

The effect of a germanium (Ge) interfacial passivation layer (IPL) on the capacitance-voltage (C-V) and current density-voltage (J-V) characteristics of TaN/HfO_2/Ge/n-InGaAs metal-oxide-semiconductor capacitors (MOSCAPs) were studied. In comparison to MOSCAPs on GaAs, the results from the accumulation region were quite similar, while the C-V curves in the inversion region were substantially different owing to the different energy bandgap. By using 8 ~ 10 Å Ge IPL and 60~70 Å HfO_2, MOSCAPs on InGaAs exhibited an equivalent oxide thickness (EOT) of ~ 11 Å and gate dielectric leakage current density (J_g) of ~ 10^{-5} A/cm^2 at V_g-V_{FB} =1 V with good C-V frequency dispersion, whereas poor electrical characteristics were obtained from the devices without a thin Ge IPL. These results show that a thin Ge IPL in optimal conditions passivates InGaAs surface effectively and provides a high quality interface.

INTRODUCTION

One of the most challenging issues in III-V compound semiconductor devices is the lack of stable nature gate oxide like SiO_2 on Si substrate [1]. Recently, by employing silicon (Si) or germanium (Ge) interfacial passivation layers (IPL), remarkable results such as small capacitance-voltage (C-V) frequency dispersion, low D_{it}, and a thin equivalent oxide thickness (EOT) with low dielectric leakage currents have been achieved on GaAs substrate [2-3]. There has been very little work on InGaAs MOSCAPs with physical vapor deposition (PVD) Ge and HfO_2, although a Ge IPL and HfO_2 dielectric have shown the possibility of effectively passivating GaAs surface to prevent it from Fermi level pinning and to provide excellent gate dielectric scalability from GaAs MOSCAPs. In this work, we present TaN/HfO_2 MOSCAPs on molecular beam epitaxy (MBE)-grown n-InGaAs layer using a thin Ge IPL.

DEVICE FABRICATION

Figure 1 shows the schematic structure of an InGaAs layer epitaxially grown on a n-GaAs substrate. The doping concentration of Si-doped $In_{0.2}Ga_{0.8}As$ was 1.0 × 10^{18}/cm^3, which was higher than that of GaAs used in this work (2.0 × 10^{17}/cm^3). Ge/HfO_2/TaN gate stacks were prepared by RF (Ge) and DC (HfO_2 and TaN) sputtering on the chemically cleaned (HCl + $(NH_4)_2S$) n-type GaAs and InGaAs samples. Post-deposition annealing (PDA) was performed at 600 °C in a N_2 (5% O_2) ambient. A gate electrode was patterned using photolithography and reactive ion etching, and the Ohmic backside contact was formed using AuGe/Ni/Au.

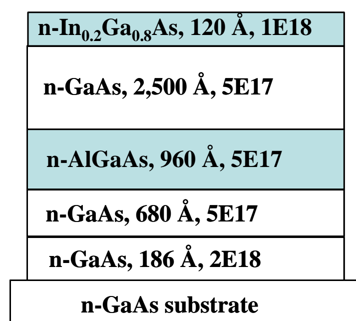
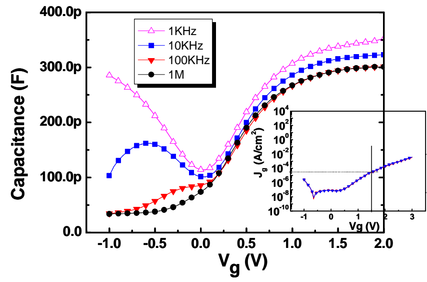


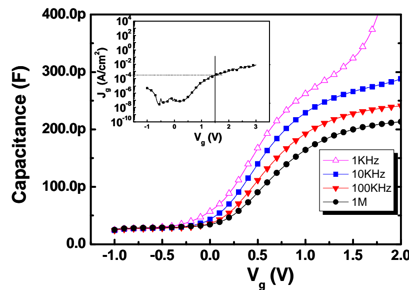
Fig. 1. The schematic structure of an InGaAs layer

RESULTS AND DISCUSSION

Figure 2 shows C-V curves with varying frequencies of the InGaAs MOSCAPs with (2a) and without (2b) a Ge IPL including the inset showing the J-V curves. In accumulation regime, higher capacitance (i.e. thinner EOT), smaller frequency dispersion and smaller J_g were obtained from the device with a Ge IPL compared to those without an IPL as in GaAs MOSCAPs [3]. Figure 3 compares C-V and J-V curves of InGaAs (3a) and GaAs (3b) MOSCAPs with an optimum Ge IPL. Both devices went through the same fabrication processes such as a surface preparation, Ge IPL, HfO_2 (~75 Å), PDA, TaN for a fair comparison. In the accumulation region, almost similar results (EOT of ~ 13 Å, J_g of ~ 10^{-6} A/cm^2) were obtained. The interface state densities (D_{it}) calculated using the conductance method for InGaAs and GaAs MOSCAPs were ~4.8 × 10^{12} and ~ 3 × 10^{12} cm^{-2}eV^{-1}, respectively.

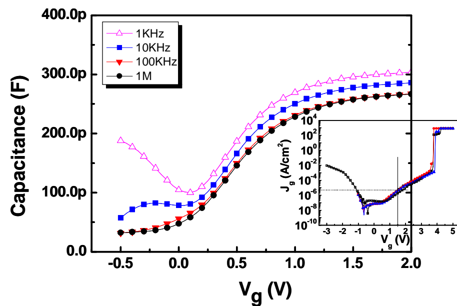


(a) MOSCAPs with a Ge IPL on InGaAs

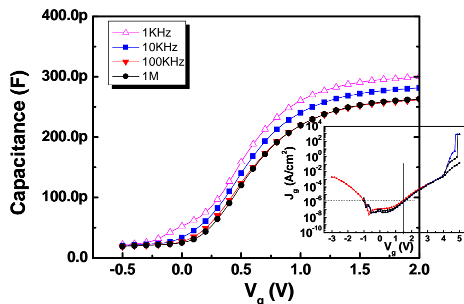


(b) MOSCAPs without a Ge IPL on InGaAs

Fig. 2. C-V curves with varying frequencies (t_{HfO2} ~ 60-70Å). The inset illustrates J-V curve.



(a) MOSCAPs with a Ge IPL on InGaAs



(b) MOSCAPs with a Ge IPL on GaAs

Fig. 3. C-V curves with varying frequencies (t_{HfO2} ~ 70-80Å). The inset illustrates J-V curve

Table I summarizes electrical properties according to process conditions. Similar to GaAs MOSCAPs [4], the results from InGaAs MOSCAPs show that a too thin Ge IPL causes large frequency dispersion indicating a poor interface quality and that a too thick Ge IPL results in smaller capacitance, which indicates a poor interface quality and/or a contribution of Ge itself as a part of dielectrics. However, the devices with optimal Ge thickness (8-10 Å) and PDA condition (600 °C 40 s) show excellent C-V and J-V characteristics representing a high quality interface. In the inversion regions, C-V curves of the MOSCAPs with and without a Ge IPL on InGaAs are striking. It is worth mentioning that as Ge thickness increases and/or PDA time at a fixed temperature lengthens, the inversion capacitance becomes larger (see $C_{inv.}/C_{acc.}$ ratios in table I). It can be explained that during process, Ga, As and/or In can out-diffuse leaving vacancies or antisite defects at the InGaAs side of the interface [5], which in turn act as recombination-generation centers, and the outdiffusion of As or Ga seems to be enhanced by a Ge layer because of the formation of an energetically favorable GeAs layer [5]. Those process-induced defects do not seem to significantly affect interface quality in the case of optimum conditions (optimal Ge thickness and PDA condition), considering the results from an optimum condition, but might deteriorate interface quality and junction leakage in metal-oxide-semiconductor field effect transistors as the Ge thickness increases and the PDA conditions become stronger. The high temperature (100 °C) measurement exhibited considerably increased inversion capacitance at the fixed frequencies indicating more minority carrier generation through these defects (Data are not shown here).

TABLE I
C-V CHARACTERISTICS OF INGAAS MOSCAPS ACCORDING TO VARYING CONDITIONS

Ge IPL	PDA	Accumulation Cap. (pF) & EOT (Å) @2V&1MHz	Inversion Cap. (pF) @-0.5V&1KHz	C_{inv}/C_{acc} (%)	Frequency Dispersion : %(%)	Frequency Dispersion : ΔV_{FB} (mV)
~0Å	500℃, 300s	165 (23)	28	17	49.7	390
	600℃, 40s	213 (17)	30	14	35.2	260
	600℃, 180s	249 (14)	132	53	18.1	150
~2-3Å	600℃, 10s	295 (11.4)	93	32	16.9	120
	600℃, 40s	293 (11.5)	136	46	12.6	80
	600℃, 300s	273 (12.4)	145	53	11.7	40
~8-10Å	600℃, 10s	289 (11.2)	181	63	9.1	70
Optimum	**600℃, 40s**	**317 (10.6)**	**216**	**68**	**7.6**	**30**
	600℃, 300s	259 (13.1)	197	76	10	50
~30-40	600℃, 10s	209 (17.6)	170	81	9.6	200
	600℃, 40s	170 (23.4)	134	79	1	40
	600℃, 300s	132	116	88	6.1	-

CONCLUSIONS

Using a Ge IPL on a MBE-grown InGaAs layer, a high-quality interface between HfO_2 and InGaAs surface has been implemented, leading to ultra-thin EOTs, excellent C-V frequency dispersion characteristics and low dielectric leakage current.

ACKNOWLEDGEMENTS

This work was partially supported by Intel Corporation.

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ACRONYMS

MOSCAP: Metal-Oxide-Semiconductor Capacitor
IPL: Interfacial Passivation Layer
C-V: Capacitance-Voltage
J-V: Current Density-Voltage
PDA: Post-Deposition Annealing
EOT: Equivalent Oxide Thickness
PVD: Physical Vapor Deposition
MBE: Molecular Beam Epitaxy