Realization of InAlN/GaN Unstrained HEMTs on SiC Substrates with a 75 Å Barrier Layer

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ABSTRACT

In this work, we describe the first reported unstrained InAlN/GaN HEMT on SiC with a 7.5 nm barrier thickness. The device reported has a gate length of 250 nm and demonstrated I_{max} = 861 mA/mm, g_{mp} = 355 mS/mm, f_t = 43 GHz, and $f_{max[MAG]}$ = 66 GHz. Power measurements for a 7.5 nm barrier device with a 250 nm gate resulted in 2.0 W/mm, 29.3% Peak PAE at X-band.

INTRODUCTION

Tremendous advances have been made in AlGaN/GaN HEMT power and frequency performance to date achieving very high current densities and high voltages [1-4]. However, these devices inherently rely on strain and spontaneous polarization to create high current densities. Common AlGaN/GaN HEMT structures use barrier thicknesses exceeding 160 Å to achieve this. Short channel effects can be observed when using these barrier thicknesses for gate lengths as large as 250 nm. As device requirements move to higher frequencies it is desirable to reduce gate lengths to 100 nm or less. Gate recesses can be used to mitigate these short channel effects. However, these recesses typically rely on a timed etch and can introduce unintended effects at the interface. Another solution is to grow the barrier layer very thin so no recess is required. However, AlGaN/GaN HEMTS rely on both piezoelectric and spontaneous polarization to obtain the required charge for power electronics. In order to achieve very high current densities in an AlGaN/GaN interface device, the AlGaN barrier layer must be as thick as 18 nm. Kuzmik has shown that InAlN/GaN interfaces have the potential to produce a large spontaneous polarization charge due to the large conduction band offset [5]. Lattice matched materials such as InAlN/GaN reduce the strain and the piezoelectric contribution to the charge in the channel. By removing strain effects from the device, the sensitivity of GaN based HEMTs to processing and growth changes can potentially be reduced. These properties should allow for thinner than usual barrier layers while maintaining high sheet charge densities.

Higashiwaki et. al. have demonstrated 6 nm InAlN layer MISHEMTs with impressive small signal performance. Their work uses a 3 nm silicon nitride layer to form a MISHEMT. Even when placing the gate at 9 nm from the channel, short channel effects are still observed in the DC-IV curves [6]. The work presented here demonstrates the ability to fabricate a HEMT with a 7.5nm InAlN barrier and a 250nm Schottky gate.

EXPERIMENT

Several InAlN/GaN HEMT structures were investigated with InAlN barrier thickness ranging from 7.5 – 18 nm while maintaining high charge density in the channel. The material was grown by Metal-Organic Chemical Vapor Deposition (MOCVD) in a close-coupled showerhead reactor by Aixtron/Thomas Swan on 6H-SiC substrates. A nucleation layer of AlN was used to transition to a GaN buffer. A thin layer (5 Å) AlN was grown before the lattice matched InAlN barrier. Three wafers were grown with progressively thinner barriers. Table 1 shows the target thickness and corresponding optically measured sheet resistance.

Approximate Barrier Thickness (nm)	18	11	7.5
Rsheet (Ω/sq)	291	306	411

Table 1 Sheet Resistance vs. InAlN Barrier Thickness

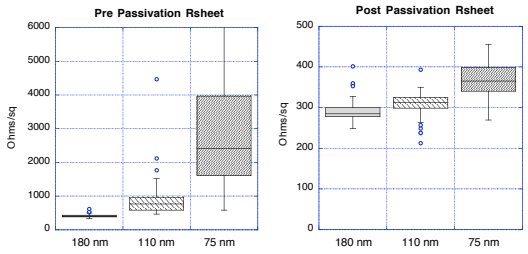
The wafers were all processed together using a standard high performance device mask, which included varying device sizes. Measurements were made at each process step. The process included mesa definition, ohmic contact formation, 1ME, e-beam gates, Si_3N_4 passivation

deposition and etch, 2ME, and bridge. Ohmic metal was a standard Ti/Al/Ni/Au stack alloyed at 850C for 30 sec. Si_3N_4 deposition was done using a PlasmaTherm 790 Plasma Enhanced Chemical Vapor Deposition (PECVD) process.

MEASUREMENTS AND DISCUSSION

Measurements were made at all steps of the process. Post ohmic alloy measurements were made using a Keithley 450 parameter analyzer. This included TLM measurements of Rsheet and contact resistance. At post gate deposition the 2 finger devices were measured using HP8510 and HP4142 network and parameter analyzers. Once passivation was complete devices were measured again as well as the PCM structures. After final front side processing all large area devices were probed.

Figure 1 compares the post alloy sheet resistance data with post passivation sheet resistance data. The sheet resistance measurements progressively went up to an extremely high value, well over 2000 Ω/sq, for the 7.5 nm barrier sample. Post passivation measurements are shown in Figure 1b. These measurements show a more acceptable sheet resistance.



a b

Figure 1 Sheet Resistance comparison Before and After Passivation

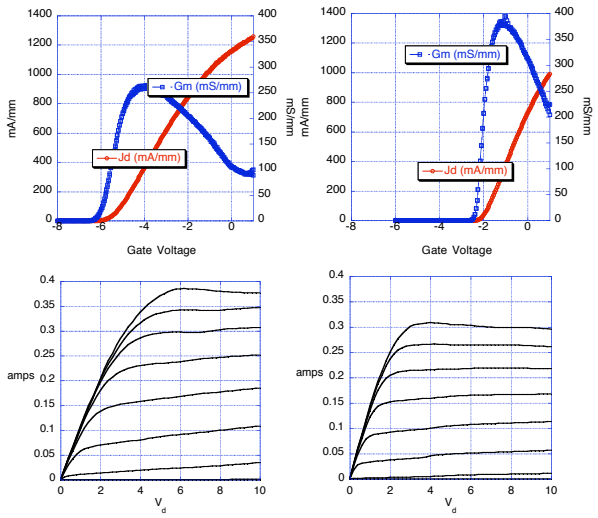
The 7.5 nm InAlN barrier sample brought the surface charge closer to the channel. The proximity of the surface charge is assumed to cause a depletion of carriers in the channel and an increase in sheet resistance. Once passivated, the charge is restored as can be seen in the reduced sheet resistance in Figure 1b.

Barrier Thicknes	Ft (GHz)	Fmax (Mag)	Gm (mS/mm)	Idss (mA/mm)	IMAX (mA/mm)	Vp (V)
75	43	66	355	604	861	-1.7
110	34	45	349	839	1040	-2.5
180	48	65	298	1108	1230	-4.4

Table 2 2x150µm Device Parameters Post Passivation

Basic device parameters measured at passivation are displayed in Table 2. These data are taken from a 2x150µm device.

It can be seen that the open channel current for the thinner sample is lower than the thicker barrier devices. Also, this current is lower than most state of the art AlGaN/GaN devices. However, g_m increases from 298 mS/mm to 355 mS/mm and f_T remains acceptable for a 250 nm gate length. Figure 2 shows the I-V curves after passivation for both 180 nm and 7.5 nm barrier thicknesses. Both of these devices had 250 nm gate lengths. The 180 nm barrier device clearly displays short channel effects. The 7.5 nm barrier device had much lower output conductance and less negative threshold voltage compared to the thicker sample.



a b

Figure 2 DC-IV Curves a) 18 nm InAlN barrier, b) 7.5 nm InAlN barrier

Load pull measurements of the 7.5 nm barrier device at 10 GHz are displayed in Figure 3. These are the first reported power measurements for 7.5 nm InAlN/GaN HEMTs. This device is an 8x100µm device with a 250 nm gate. The device was biased at V_{DS} = 20V and V_{GS} = -2.2 V. The results were 1.7 W/mm and 10 dB gain at peak PAE of 29%. The peak power was 2.0 W/mm and small signal gain of 14 dB. The devices were matched for power.

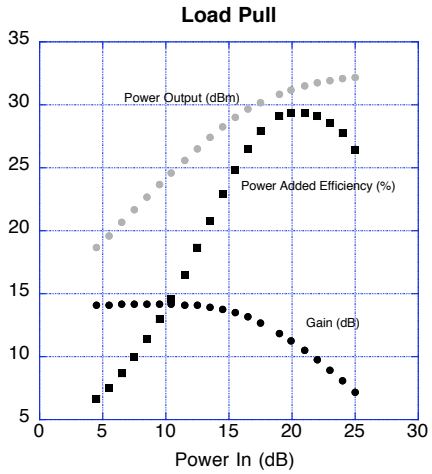


Figure 3 Load pull results for 7.5 nm InAlN barrier 800µm device at 10 GHz.

CONCLUSION

As mentioned earlier, AlGaN/GaN devices require a minimum thickness barrier to produce the amount of charge needed for high power applications. This thick barrier limits the frequency response that can be achieved due to short channel effects. InAlN/GaN device structure has been discussed as a potential nitride based material system to reduce the barrier thickness limitations. [5] We have shown results from three wafers grown with varying InAlN thicknesses, 7.5 nm, 11 nm and 18 nm. The results show an improvement in short channel effects. These first devices demonstrated acceptable frequency response and exceptional gain. Plans are to optimize the growth and device design to improve open channel current and frequency response.

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