High Frequency Noise Characterization and Modeling of InGaP/GaAs SHBTs

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Abstract: InGaP/GaAs SHBTs have been fabricated and the device RF and noise performance has been measured. A small-signal model has been created from the S-parameters of the measured devices. Thermal and shot noise is added to create a first generation noise model, which shows good agreement with measured data. The devices (L=3x12 μm^2) showed an F_{MIN} = 1.68 dB at 6 GHz for V_{CE} = 1.8 V and I_C = 1.56 mA.

1. Introduction

InGaP/GaAs HBTs have become the dominant device technology for cellular phone power amplifiers due to their high linearity, high output resistance, and ability to sustain high current densities; However, InGaP/GaAs HBT's have not been used as low noise amplifiers due to the high noise figures.

Due to the emphasis on the noise performance of a transistor, predicting the scaling trends for noise would be useful. Additionally, the ability to predict the noise figure of a device would provide a better picture when designing either the device layouts or the layer structure. Despite the advantages of investigating noise in this material system, there have been few reports of noise performance on these devices [1-4].

This work creates a small-signal model from S-parameters and from that model, a first-generation noise model is used to analyze the noise performance. The model investigates the separate contributions to the total noise of the transistor each individual noise component.

2. Layer Structure and Device Fabrication

A standard InGaP/GaAs SHBT layer structure was used in this study. The emitter consisted of an InGaAs layer on the surface that is graded to GaAs, and an InGaP layer at the emitter and base junction. The base was a heavily p-type doped GaAs layer and the collector was lightly doped n-type GaAs. The subcollector was made from GaAs and was heavily n-type doped.

The layout used in this study was a high-speed layout developed at the University of Illinois. The baseline process is described in [5]. All three metals were defined by electron-beam lithography. The emitter metal was Ti/Pt/Au and was used as the mask for the emitter-etch. InGaAs, GaAs, and InGaP were etched away using selective wet etches and Ti/Pt/Au was deposited for the self-aligned base contact. A timed etch was used to etch down to the sub-collector, and AuGe/Ni/Au was deposited on the subcollector. The device was then annealed to reduce the collector contact resistance. BCB was spun-on to passivate and planarize the device, then etched to reveal the device contacts. Finally, a thick metal layer was deposited to produce the probe pads. A top-down view of this structure before planarization is included in fig 1.

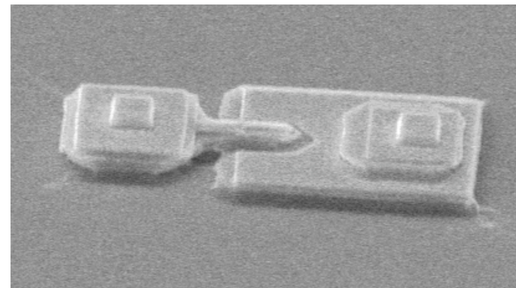


Fig. 1: Top down views of a transistor before planarization.

3. Device Measurement and Modeling

The RF measurement was done using an HP 8510C VNA, and a HP 4142B DC power source. The calibrations were done using a standard on-wafer SOLT calibration.

Noise figure measurements were performed on wafer from 2 GHz to 24 GHz using ATN solid state tuners, an Agilent N8975A noise figure meter, and an Agilent E8364A Network Analyzer at an ambient temperature of 21°C. S-parameter calibration was performed using on-wafer SOLT calibration standards. Noise calibration also used on-wafer

standards. At each bias and frequency condition, the noise figure was measured at 16 different source input impedance states. The F_{MIN}, R_N, and Γ_{OPT} were extracted from this measured data using ACCO-USA (now Maury Microwave) NP5 software.

The device model used in this study was a standard π-model for the HBT and is shown in figure 2. The values for C_{JE}, R_{BE}, and G_M were calculated from [6]. R_E wase calculated from [7]. The total base-collector capacitance was calculated from [8] and the ratio was calculated from geometry. The extrinsic and intrinsic base resistance values as well as R_C were optimized with their starting values determined through geometry. The most pertinent small-signal parasitic components are listed in table 1.

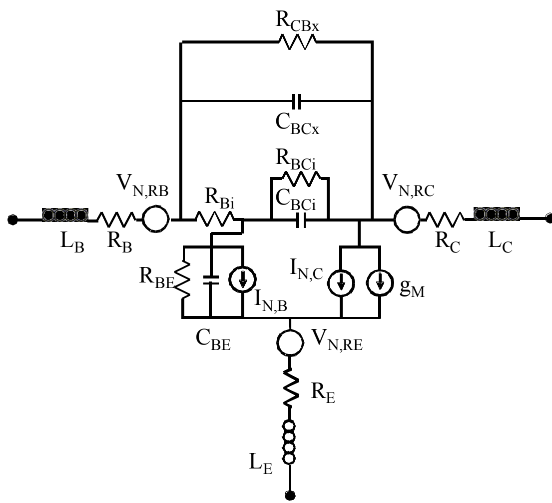


Figure 2: Small-signal noise model of the device.

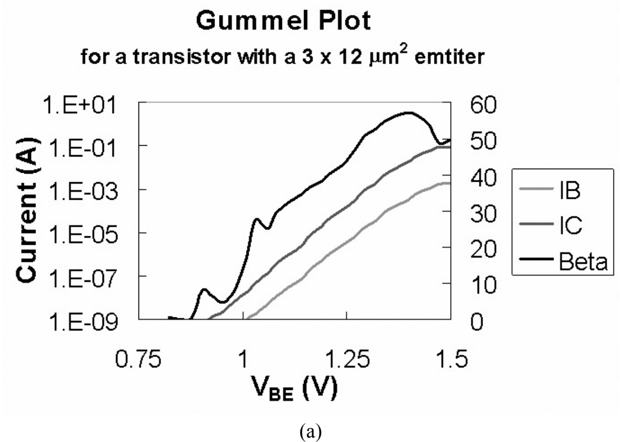
The thermal noise for the resistors and the shot noise currents for the base and collector junctions were calculated from [9]. They are schematically represented by the current sources and voltages sources with a subscript N, such as $V_{N,RB}$ acting as the voltage noise for the base resistance. The thermal noise is modeled as a random noise source with a rms value of $V_N = \sqrt{4 * k * T * R}$. The shot noise is modeled as a random current source with a rms value of $I_N = \sqrt{2 * q * I}$. The noise from the capacitors and inductors was negligible. Due to low currents, the junction temperature was assumed to be room temperature (21°C).

4. Results and Discussion

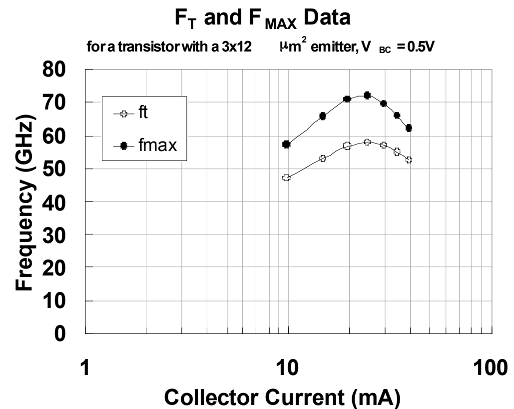
The DC and RF parameters of the device are shown in figure 3. The device had a β of 57, an f_T = 57 GHz, and an f_{MAX} = 72 GHz. The BV_{CEO} of this device was 8.2V.

	Extracted Parameters	Calculation Method
R_B (Ω)	8.33	Geometry
$R_{B,I}$ (Ω)	1.4	Geometry
R_E (Ω)	4	S-parameters (Ref 7)
$R_{BE,I}$ (Ω)	806	S-Parameters (Ref 6)
R_C (Ω)	4	Geometry
$C_{BC,I}$ (fF)	33.44	S-Parameters (Ref 8), Geometry
$C_{BC,Ex}$ (fF)	27	S-Parameters (Ref 8),

Table 1: Device parasitic parameters used in the model and the method of calculation.

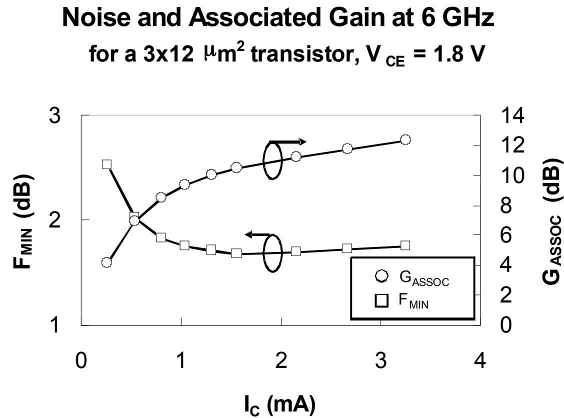


(a)

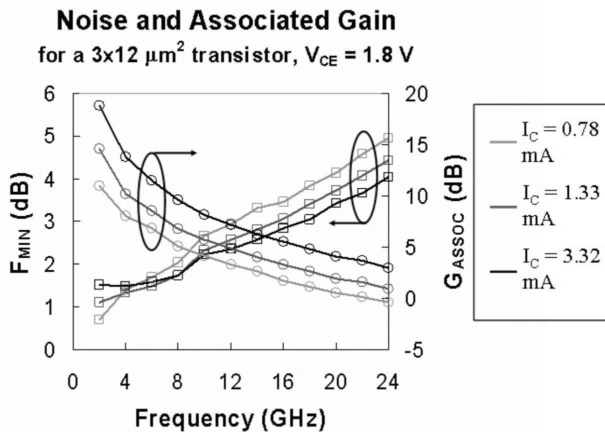


(b)
Figure 3: (a) Gummel and (b) f_T and f_{MAX} properties for a 3x12 μm² transistor.

The measured noise parameters at 6 GHz at different bias points is included in figure 4. The noise values were taken at 6 GHz. The devices show F_{MIN} of 1.68 dB at 6 GHz for V_{CE} = 1.8 V and I_C = 1.56 mA.



(a)



(b)
Figure 4: a) F_{MIN} and G_{ASSOC} plotted for a transistor with a 3x12 μm emitter taken at 6 GHz and b) F_{MIN} and G_{ASSOC} plotted against frequency for three different bias points

The measured and modeled noise figures vs. frequency for one bias point, V_{CE} = 1.8V and J_C = 3.125 kA/cm², are plotted in figure 5. The measured and modeled data show good agreement, indicating that the majority of the noise can be modeled as shot noise or as thermal noise. It should be noted that the model does not include any low-frequency noise components.

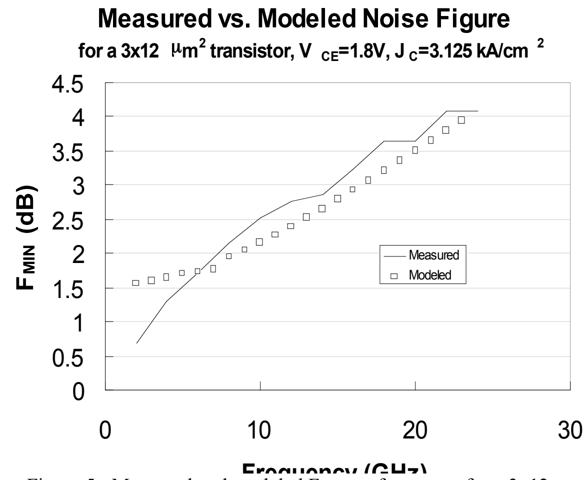


Figure 5: Measured and modeled F_{MIN} vs. frequency for a 3x12 mm2 transistor with V_{CE} = 1.8 V and J_C = 3.125 kA/cm².

The contributions of the three different calculated noise terms are included in figure 6. The collector shot noise is the dominant noise term, followed by the thermal noise and the base shot noise. It should be noted that while the collector shot noise is derived from the collector current, it can still be further minimized through optimization of the layer structure and device layout. For example, a reduction in extrinsic emitter resistance would yield a decrease in F_{MIN} generated by the collector current from 3.05 dB to 2.8 dB at 20 GHz.

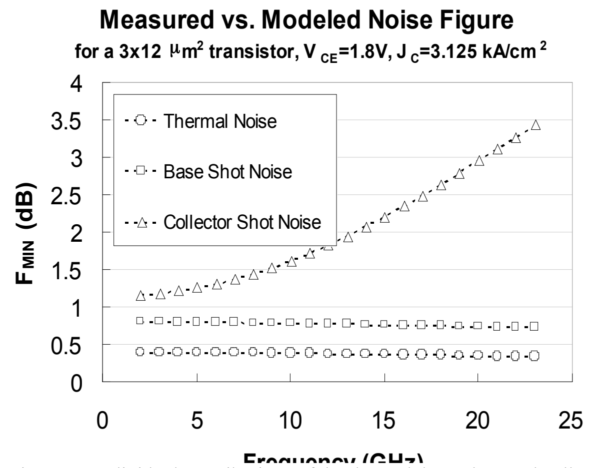


Figure 6: Individual contributions of the thermal, base shot, and collector shot noise examined.

4. Conclusion

InGaP/GaAs SHBTs have been fabricated and their DC, RF, and noise characteristics have been measured. From the S-parameters, a small-signal model has been created. Thermal and shot noise is then added to the model, showing good agreement between the modeled and measured noise figures. Finally, the model is used to analyze the

contributions to the noise from each of the major noise sources and indicates that the largest contributor to the noise figure is the collector shot noise.

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ACRONYMS:

rms = Root Mean Square
f_T: Cutoff frequency
f_{MAX}: Maximum Oscillation Frequency
HBT: Heterojunction Bipolar Transistor
SHBT: Single Heterojunction Bipolar Transistor
f_{MIN}: Minimum Noise Figure
BV_{CEO}: Breakdown Voltage between Collector and Emitter with Base open.
β: Current Gain
$C_{BC,I}$: Intrinsic Base-collector capacitance
$C_{BC,EX}$: Extrinsic Base-collector capacitance
L_E, L_C, L_B: Emitter, Collector, or Base Inductance
R_{EE}: Extrinsic Emitter Resistance
R_C: Collector Resistance
R_{BE}: Emitter Junction Resistance
R_B: Emitter-Base Spacing Resistance
R_{BI}: Internal Base Resistance