Leakage Current Screening for AlGaN/GaN HEMT Mass-Production

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Abstract

There are defects on GaN HEMT epitaxial wafers due to defects on the SiC substrates. These defects cause large leakage current and degradation of RF performance of the devices on them. Therefore, it is very important to screen the chips on defects on the wafer in AlGaN/GaN HEMT mass-production. Through the various on-wafer DC parameters measurement, we confirmed the distribution of drain leakage current at pinch off region and their correlation with the defects on the wafers. The difference of the drain leakage current is sufficient enough to screen the defect chips at on-wafer DC probing test. With this screening procedure, we can maintain reliable and stable mass production of AlGaN/GaN HEMTs.

INTRODUCTION

Recently, AlGaN/GaN HEMTs have received much attention for microwave high power applications, such as wireless base stations and radars, since they have suitable device performance owing to the excellent material properties [1-2]. Eudyna has successfully developed 50V operation AlGaN/GaN HEMTs, released Engineering Samples in 2005 and moved into mass-production in 2006 [3]. However there are still a certain number of defects on the SiC substrates due to their growth immaturity. The defects cause large leakage current and degradation of RF performance of the devices. Therefore the screening of chips on the defects becomes a critical issue at the shift from sample-level production to actual mass-production. There are few reports studying the correlation between the gate leakage current and substrate defects [4].

In this paper, we investigate the leakage current of the defect chips in detail and show the effective screening procedure of defect chips utilizing the drain leakage current measurement.

FET STRUCTURE AND EPITAXIAL WAFER

Figure 1 shows the schematic cross sectional view of our AlGaN/GaN HEMTs. The source and drain electrodes are fabricated of evaporated Ti/Al with recessed ohmic technology. The gate electrode consists of Ni/Au, and SiN passivation was deposited on the n-GaN cap layer using plasma CVD [5].

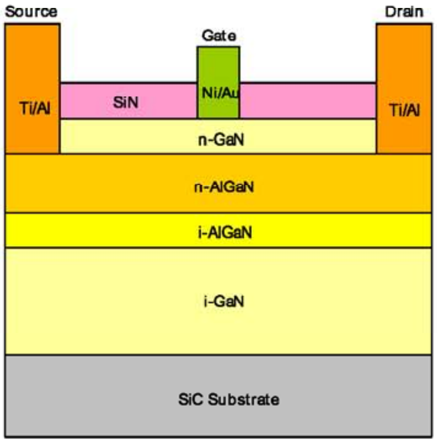

Fig.1 Schematic cross section of AlGaN/GaN HEMT

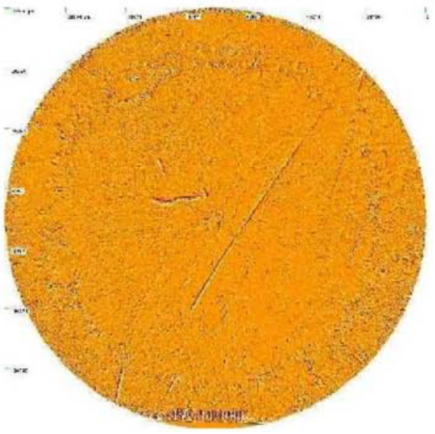

Fig.2 Surface morphology image of 3-inch epitaxial wafer on SiC substrate

The epitaxial layers of HEMT were grown by MOCVD on 3-inch semi-insulating SiC substrates. Figure 2 shows the surface morphology image of the epitaxial wafer on SiC substrate. This image taken by the optical surface analyzer was provided by Hitachi Cable Ltd. It can be seen some lines and area of defects such as micropipes, hexagonal pits and contamination-induced defects on the epitaxial wafer. The detail visual inspection indicates these lines are made of many defects. We confirmed these defects cause the increase of the leakage current and the degradation of RF performance of the devices, thus screening of chips on the defects is inevitable at the mass production process.

SCREENING PROCEDURE AND ANALYSIS

In our AlGaN/GaN HEMT wafer process, we carry out the on-wafer DC probing test for every single die, and measure various DC parameters such as forward breakdown voltage (Vgsf), reverse gate-source leakage current (Igso), reverse gate-drain leakage current (Igdo), pinch off voltage (Vp), and drain leakage current at pinch off region. Among these DC parameters, we investigated which parameter gives most efficient screening procedure of the defect chips.

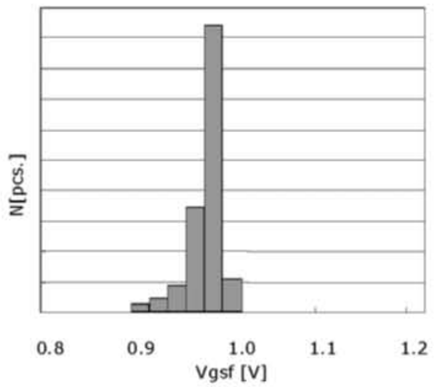

Fig.3 (a) Distribution data of forward breakdown voltage (Igs=0.1mA/mm)

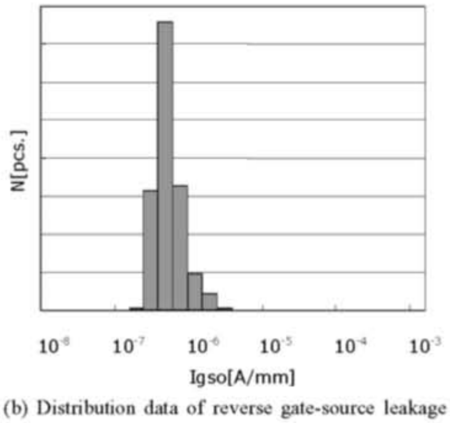

Fig.3 (b) Distribution data of reverse gate-source leakage current (Vgs=-10V)

Figure 3(a-e) show the distribution of measured DC parameters of the AlGaN/GaN HEMTs on the particular epitaxial wafer shown in Figure 2. The gate length and width are 0.9um and 11.3mm, respectively. Among these data, the distribution of drain leakage current (Figure 3(e)) suggests an existence of normal chips and abnormal ones. The drain leakage current of normal chips are less than about 10^{-6}A/mm, on the other hand, one of abnormal chips distribute between 10^{-6}A/mm and 10^{-4}A/mm. We couldn't see significant difference in any other DC parameters except for the drain leakage current.

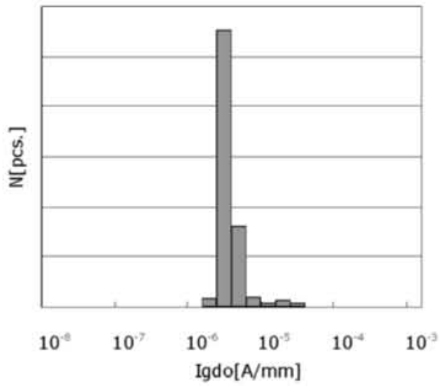

Fig.3(c) Distribution data of reverse gate-drain leakage current (Vgd=-50V)

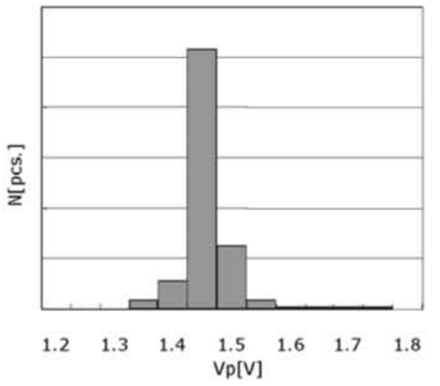

Fig.3(d) Distribution data of pinch off voltage (Vds=15V, Ids=0.1mA/mm)

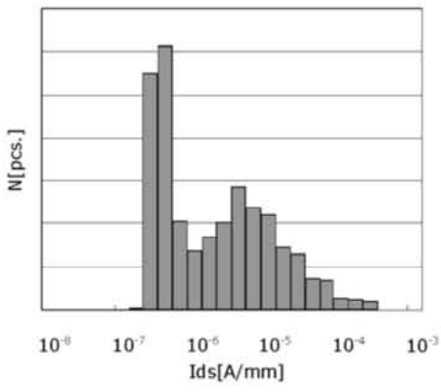

Fig.3(e) Distribution data of drain leakage current (Vgs=-3V)

Figure 4 shows the map of the drain leakage current of the AlGaN/GaN HEMT chips at the on-wafer DC probing test, which were discussed in the above . Red marks indicate abnormal chips which have the drain leakage current of greater than 10^{-6} A/mm. The area of large drain leakage current of the map clearly corresponds to the area of defects on the wafer image shown in Figure 2. It suggests the drain leakage current of chips with defects is larger than ones without defects.

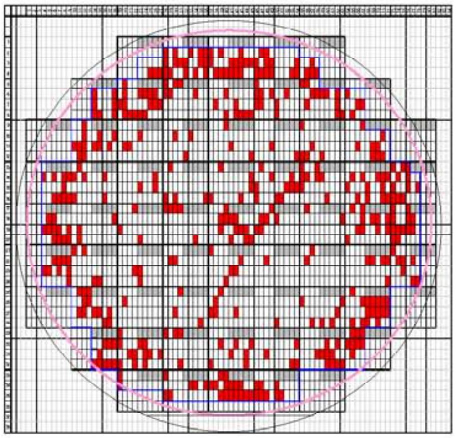

Fig.4 Map of the drain leakage current of on-wafer DC probing test

The DC characteristics of defect chips and non-defect chips were investigated in detail. Figure 5 shows sub-threshold characteristics of the both chips. There is no significant difference in gate leakage current of either the defect or non-defect chips. However, the drain leakage current of the defect chip is obviously larger than one of the non-defect chip. It suggests that the large drain leakage current of defect chips is due to drain-to-source leakage current not drain-to-gate leakage current.

Figure 6 shows the photograph of a typical hexagonal pit observed at the defect chip on the epitaxial wafer. Through the observation of the defect part by scanning electron microscope (SEM) shown in Figure 7, it was observed the abnormal epitaxial growth caused by the defect of the SiC substrate. We believe this abnormal epitaxial growth leads poor pinch off characteristic and large drain-to-source leakage current. A difference of drain leakage current is large enough to screen the defect chips at on-wafer DC probing test.

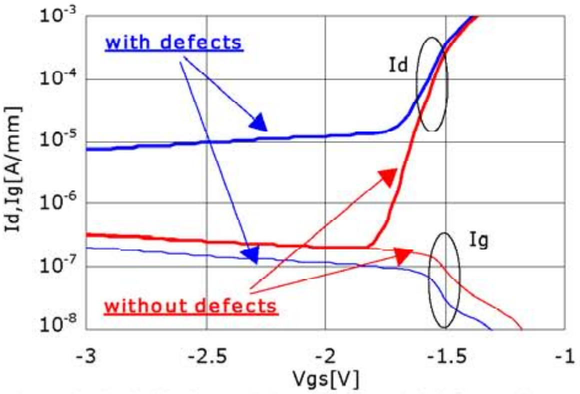

Fig.5 Sub-threshold characteristics of a chip with defects and one without defects

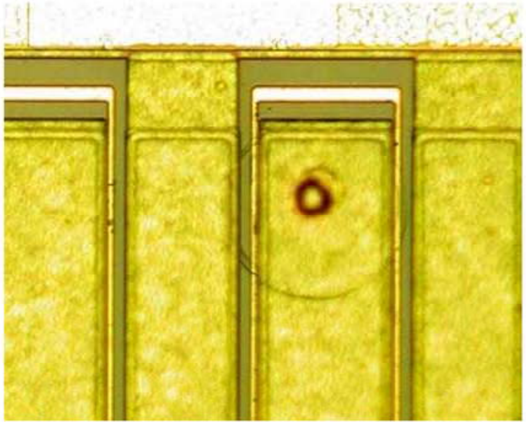

Fig.6 Microscope image of a hexagonal pit on epitaxial wafer

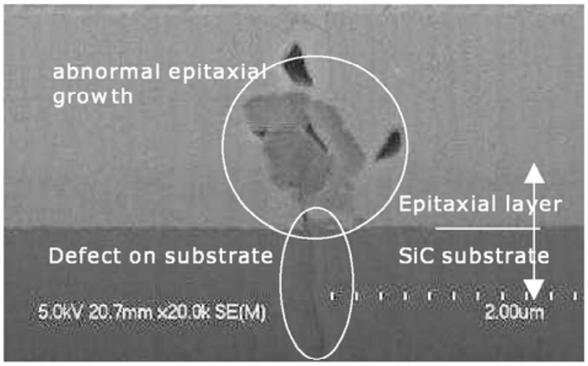

Fig.7 SEM image of a hexagonal pit on epitaxial wafer

CONCLUSION

We carried out on-wafer DC probing test for the AlGaN/GaN HEMTs and confirmed the distribution of drain leakage current at pinch off region and its good relation with the defects on the substrate. The drain leakage current is a very useful parameter to screen the defect chips. With this screening procedure, we can maintain reliable and stable mass production of AlGaN/GaN HEMTs.

ACKNOWLEDGEMENTS

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REFERENCES

[1]A.Maekawa et al., A 500W Push-Pull AlGaN/GaN HEMT Amplifier for L-Band High Power Application, 2006 IMS Symposium Digest, pp.722-725.
[2]Y.Tateno et al., GaN HEMT for W-CDMA and WiMAX Base Station Application, 2006 IMS Symposium Workshop(WSM) Digest, pp.132-143.
[3]E.Mitani et al., Mass-Production of High-Voltage GaAs and GaN Devices, 2006 CS MANTECH Digest, pp.183-186.
[4]K.Matsushita et al., Gate Leakage Current of AlGaN/GaN HEMTs Device Influenced by Substrate Defects, 2005 CS MANTECH Digest, pp.71-73.
[5]J.Nikaido et al., A Highly Uniform and Reliable AlGaN/GaN HEMT, 2005 CS MANTECH Digest, pp.151-154.

ACRONYMS

HEMT: High Electron Mobility Transistor
CVD: Chemical Vapor Deposition
MOCVD: Metal Organic Chemical Vapor Deposition