

# Failure Mechanisms in GaN HFETs under Accelerated RF Stress

A.M. Conway, M. Chen, P. Hashimoto, P.J. Willadsen, and M. Micovic

HRL Laboratories, LLC  
3011 Malibu Canyon Dr. Malibu, CA 90265  
(310) 317-5302; fax: (310) 317-5450; e-mail: [mmicovic@hrl.com](mailto:mmicovic@hrl.com)

**Keywords:** GaN, HFET, reliability, life test, failure mechanisms

## Abstract

This work reports the results of the comprehensive three temperature accelerated RF life test on GaN HFETs at 10 GHz. An activation energy of 1.8 eV was extracted giving a MTF at  $T_{ch} = 125^\circ\text{C}$  of  $3.5 \times 10^9$  hours. Electrical characterization and cross sectional TEM were performed on devices that gracefully reached failure criteria. No visible evidence of gate sinking or electro migration was observed. Pulsed I-V measurements show an increase in “current slump” phenomena most likely caused by an increase in surface states between the gate and drain was the main cause of device failure. FIB/TEM was also performed on devices stressed in air which show feature on drain edge of gate in the AlGaN barrier layer. EELS maps show increased oxygen levels in the defect region.

## INTRODUCTION

GaN devices have been the subject of intense research for the past decade. Due to its wide band gap, high breakdown field, current density, and saturated velocity, this material system is well suited for high temperature and high power applications from microwave to millimeter-wave frequencies [1]. Much progress has been made in improving device performance to the extent that researchers have reported record numbers for channel charge density and power density exceeding  $2 \times 10^{13} / \text{cm}^2$  and 30 W/mm at 4 GHz [2], respectively. These extreme operating conditions along with the relative immaturity of the technology demand a closer look at the reliability of GaN devices under real life operating conditions.

## DEVICE UNDER TEST

The devices tested in this work were AlGaN/GaN/AlGaN DHFETs grown and fabricated at HRL Laboratories. The devices were grown by plasma assisted MBE on semi-insulating SiC substrates. The layer structure is described in detail in reference [3]. The transistors evaluated in this study have a millimeter-wave field plate gate with a gate foot length of 0.15  $\mu\text{m}$  and gate width of 200  $\mu\text{m}$ . The process includes surface passivation with  $\text{Si}_x\text{N}_y$ . The maximum device  $f_T$  at drain bias of 25 V is 50 GHz and  $f_{max}$  is 120 GHz. These devices are optimized for operation in Ka-band (26.5 GHz – 40 GHz) and exhibit power density of 5 W/mm with associated PAE of 40 % at a frequency of 30 GHz and a drain bias of 28 V. At 10 GHz and  $V_{ds} = 25$  V

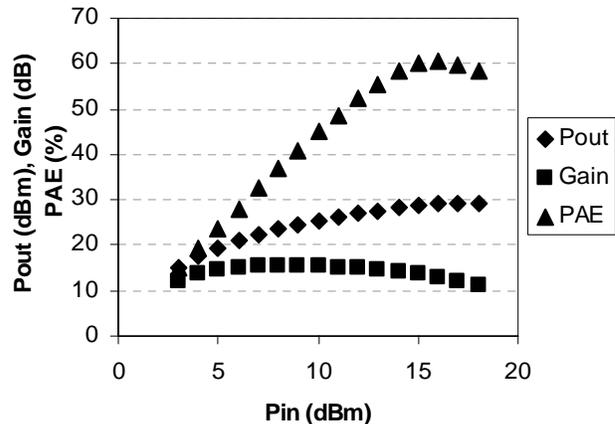


Figure 1. Representative single tone power sweep data for DUTs, biased at  $V_{ds} = 25$  V and  $I_{ds} = 20$  mA at 10 GHz.

and under optimum PAE matching conditions, the device saturated output power is 4.1 W/mm with 64 % PAE, while at  $V_{ds} = 40$  V,  $P_{sat} = 8.15$  W/mm with 56 % PAE, figure 1.

## TEST SYSTEM SETUP

Two experiments were performed on the devices described in the previous section. The first was an accelerated DC only experiment performed in air at a  $V_{ds}$  of 30 V. The second experiment, combined DC and RF stimulus at a  $V_{ds} = 25$  V and at an input RF power necessary to drive the devices into 2 dB compression at temperature. The RF life test was performed using an accelerated RF life test system configured for operation at 10 GHz and in a dry  $\text{N}_2$  environment.

The diced devices were individually mounted on gold plated copper carriers using Au80Sn20 eutectic solder then attached to a test fixture. For the DC experiment stabilizing resistors were placed in the gate bias line. For the DC+RF experiment, the matching circuits were tuned for maximum output power. The test fixture includes the heater stage, interface for DC and RF stimulus and RF input and output matching circuits. The fixture is configured in such a way that the matching circuits are physically separated from the heater stage so that only the DUT is at elevated temperature. Also, embedded in the system is an HP 4142 semiconductor parameter analyzer (SPA). Computer control allows for

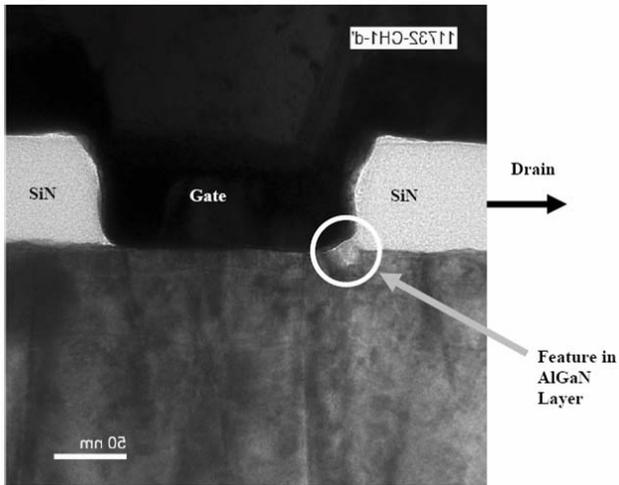


Figure 2. TEM cross section of a device that gracefully degraded under stress at  $T_{ch} = 218\text{ }^{\circ}\text{C}$ ,  $V_{ds} = 30\text{ V}$  during operation in air.

automated temperature control, data capture and in situ device characterization.

## RESULTS AND DISCUSSION

### DC Only Life Test Results

For the DC only experiment, the transistors were biased at  $I_{ds} = 40\text{ mA}$  and  $V_{ds} = 30\text{ V}$  at a channel temperature of  $172\text{ }^{\circ}\text{C}$ . Periodically the devices were cooled down to room temperature and  $I_{ds}$  versus  $V_{gs}$  curves at  $V_{ds} = 10\text{ V}$  were measured from which  $I_{dss}$  and peak  $g_m$  were extracted. After 3000 hours of stress,  $I_{dss}$  had been reduced by 10% and peak  $g_m$  was reduced by 15%.

FIB cross sections of devices stressed for 3000 hours of DC stress at  $T_{ch} = 172\text{ }^{\circ}\text{C}$  and control samples were prepared and TEM was performed in the active area of the devices.

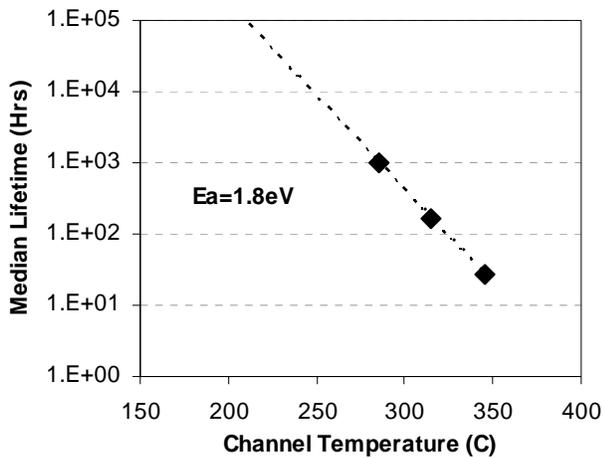


Figure 4. Arrhenius plot for activation energy extraction.

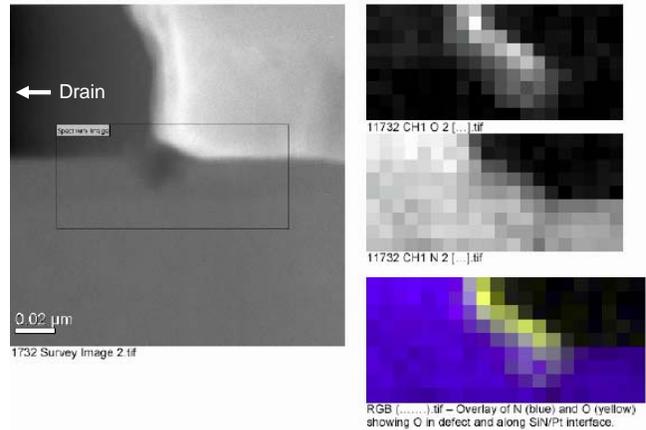


Figure 3. Electron Energy Loss Spectroscopy (EELS) maps of oxygen and nitrogen distribution of a defect shown in TEM cross section. The area of EELS scan is highlighted by the square in the left image. Oxygen distribution (Top Right), Nitrogen distribution (Middle Right), combined Nitrogen (blue) and Oxygen (yellow) map (Bottom Right).

The area around the gate edges as well as in the access regions and contact ohmic contact areas were closely investigated. The resulting images of the region underneath the gate are shown in figures 2. A distinct feature is evident in the AlGaN Schottky barrier layer on the drain side of the gate. Electron energy loss spectroscopy (EELS) maps of oxygen and nitrogen distribution of the defect shown in TEM cross section show that degradation is caused by oxidation of AlGaN Schottky barrier layer, figure 3. There was no evidence of gate sinking or electromigration of ohmic metal.

### RF Life Test Results

Six devices at each channel temperature of  $285\text{ }^{\circ}\text{C}$ ,  $315\text{ }^{\circ}\text{C}$  and  $345\text{ }^{\circ}\text{C}$  were used in this experiment. From an Arrhenius plot of the MTTFs for each channel temperature,

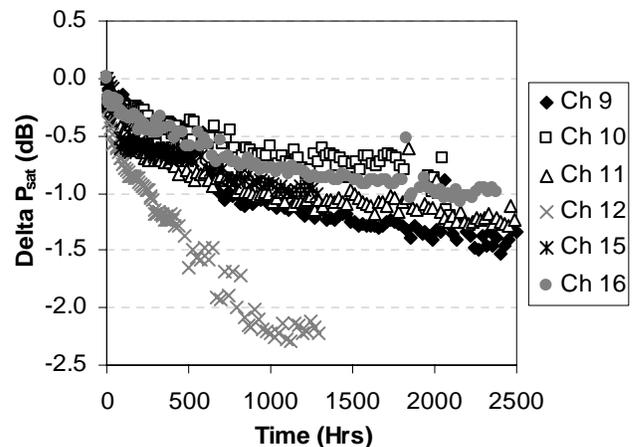


Figure 5. Saturated output power versus time for devices at a channel temperature of  $285\text{ }^{\circ}\text{C}$ .

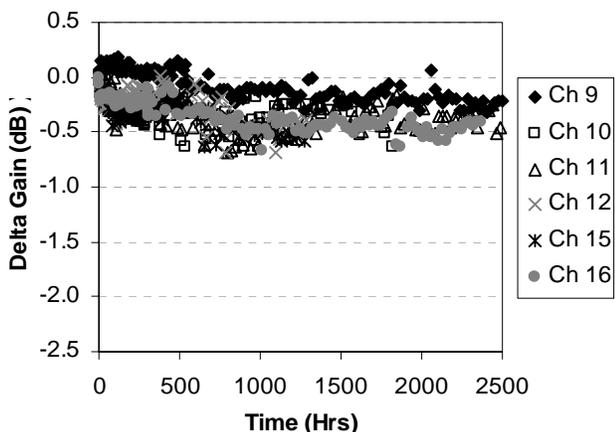


Figure 6. Change in small signal gain at a fixed input power versus time for devices at a  $T_{ch}$  of 285 °C.

an activation energy of 1.80 eV was extracted, figure 4. Using this activation energy a MMTF at a channel temperature of 125 °C is calculated to be  $3.5 \times 10^9$  hours.

The trends were similar for each channel temperature, therefore for conciseness, only the results at  $T_{ch} = 285$  °C will be discussed in detail. The saturated output power as a function of accumulated time under stress is shown in figure 5 for  $T_{ch} = 285$  °C. The devices exhibit gradual power degradation with 50 % of the devices reaching the failure criterion after 1000 hours. The maximum decrease in  $P_{sat}$  is almost 2.5 dB and the all devices reached the failure criterion of 1 dB reduction after 2500 hours of cumulative stress. By defining  $P_{sat}$  using a gate current metric (as opposed to at a fixed input power),  $P_{sat}$  is not pinned to changes in small signal gain. The change in small signal gain is shown in figure 6 and is less than 0.5 dB for all devices over the entire life test. Figure 7 displays the percent change in  $I_{dmax}$  versus time as measured at  $V_{gs} = 1$  V and  $V_{ds} = 10$  V at a baseplate temperature of 60 °C. The change in  $I_{dmax}$  ranges from 0 to 10% reduction after 2500 hours. The reduction in maximum drain current correlates

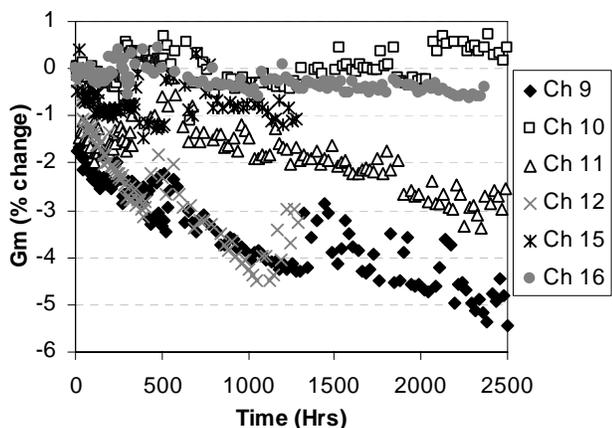


Figure 8. Percent change in  $g_m$  versus time for devices stressed at  $T_{ch}$  of 285 °C.

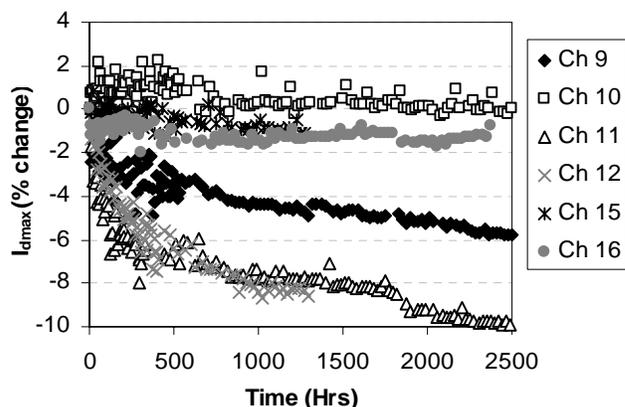


Figure 7. Percent change in  $I_{dmax}$  versus time for six devices stress at the 2 dB compression point at  $V_{ds} = 25$  V for  $T_{ch} = 285$  °C.

with a positive shift in threshold voltage. The change in peak  $g_m$  ranges from +1 % to -5 %. A complete discussion of the RF life test results can be found in [4].

FIB cross sections of failed devices and control samples were prepared and TEM was performed in the active area of the devices. The area around the gate edges as well as in the access regions and contact ohmic contact areas were closely investigated. There was no evidence of gate sinking, ohmic contact electromigration or formation of features at the drain edge of the gate as seen in the samples stressed in air.

#### Pulsed I-V

The reduction in maximum DC drain current is not enough to explain the 1 dB decrease in output power. Pulsed I-V measurements were also performed on a control sample and a stressed device at a quiescent bias point of  $V_{ds} = 25$  V and  $V_{gs} = -2$ , which are the same bias conditions for the power measurements, with a pulse width of 200 ns and a pulse separation of 1 ms. The resulting DC and pulsed I-V curves are shown in figure 9. Under pulsed conditions, trapped electrons cannot react to changes bias. The stressed

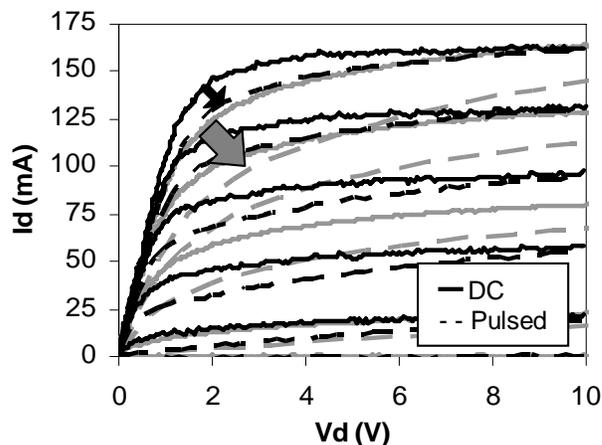


Figure 9. DC and Pulsed I-V curves for control and stressed device.

device shows a much larger decrease in knee current and increase in knee voltage which reduces the maximum current and voltage swings thus decreasing  $P_{sat}$ . It is likely that electrons, either via surface conduction from the gate or accelerated over the AlGaIn potential barrier to the surface from the channel, become trapped in surface states between the gate and drain, which partially depletes the underlying channel thus increasing  $R_{ds}$  and decreasing output power. It is speculated that during extended DC, RF and temperature stress, high electric fields between the gate and drain induce the creation of additional surface states compared to the unstressed condition.

#### SUMMARY AND CONCLUSIONS

Two accelerated reliability experiments were performed on GaN based HFETs. A three temperature accelerated RF life test was also performed on GaN HFETs at 10 GHz. From the median lifetime for each channel temperature, an activation energy of 1.80 eV was extracted which corresponds to an extrapolated MTTF at a channel temperature of 125 °C to  $3.5 \times 10^9$  hours. No evidence of gate sinking, electromigration or oxidation was visible in these devices using cross sectional TEM. Pulsed I-V measurements show an increase in current slump phenomena, most likely caused by an increase in surface states between the gate and drain, was the main cause of device failure under DC and RF stress in  $N_2$ . After 3000 hours of DC stress in air at elevated temperature, a feature on the drain edge of the gate was observed via TEM and determined to be oxidation of the AlGaIn layer. This data suggests that there are different failure mechanisms for devices operating in air and those operating in an inert environment. The use of hermetically sealed packaging or device encapsulation may significantly improve the reliability of GaN HFETs.

#### ACKNOWLEDGEMENTS

This work was supported by DARPA, project manager Mark Rosker, and managed by Lois Kehias of the Sensors Directorate of the Air Force Research Laboratory, USAF, Wright Patterson AFB OH 45433-6543.

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#### ACRONYMS

HFET: Heterojunction Field Effect Transistor  
DHFET: Double Heterojunction Field Effect Transistor  
MBE: Molecular Beam Epitaxy  
MTTF: Mean Time To Failure  
TEM: Transmission Electron Microscopy  
FIB: Focused Ion Beam  
EELS: Electron Energy Loss Spectroscopy