Surface Preparation Study in GaAs HBT Process

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Abstract:

We report the results of an experiment to investigate the impact of surface cleaning methods on the HBT base-collector turn-on voltage and transistor reliability. This experiment indicates that NH_4OH based solution is an appropriate surface preparation method for processing GaAs based HBTs. Deviation from this cleaning procedure (no clean, DI water clean or acetic acid clean) degrades the device performance and reliability. This is consistent with previous finding in literature that NH_4OH based solution produces a cleaner, more stoichiometric GaAs surface resulting in better device performance.

INTRODUCTION

Surface preparation is an important step in semiconductor device processing. Surface/interface impurities can affect adhesion properties or introduce surface states which lead to device performance degradation, such as high surface recombination velocity or high leakage current.[1,2] Thus, a contamination free, stabilized surface is essential for well behaved devices.[3] A proper surface cleaning procedure is a key element to successfully fabricating reliable, high quality semiconductor devices.

At Skyworks Newbury Park GaAs HBT fab, we recently observed device failures that were related with the surface cleaning procedure. The devices were first identified at PCM measurement by a low base-collector (BC) diode turn on voltage. Subsequent transistor level reliability testing showed that these devices have shorter stress lifetime (early wear out failure). The root-cause was traced to a surface cleaning step after the formation of base pedestal and before deposition of silicon nitride passivation (our HBTs are manufactured using a standard double mesa process).

This surface preparation step takes place in wet clean benches that house multiple baths of different chemicals. Some of these baths are shared at different process steps between wafers with or without photo resist. Such manually operated baths are susceptible to human errors (or mis-processing). Many factors can contribute to failures: using the wrong bath, filling the correct bath with the wrong chemicals, wrong bath composition, cross contamination, and bath aging, etc.

In this paper we report the results of the experiment we performed to investigate the impact of different surface cleaning methods on HBT BC diode turn-on voltage and transistor reliability. The purpose of this experiment was to explore the elimination of this surface cleaning step, removing potential process errors, or modification of the cleaning procedure to improve process margin. We also used this experiment to find out if we need to increase bath change out frequency or dedicated baths are required in order to minimize cross contamination.

EXPERIMENTAL

The experiment was a custom DOE design with 1 factor (clean) at 9 different levels. A total of 18 runs (with duplicates) plus 2 extra runs were performed. The wet clean process splits consist of NH_4OH solutions with different concentration (2%, 8% and 15%), aged or fresh, and with or without plasma ash. They were compared to other cleaning methods such as acetic acid clean, DI water clean and no clean. HCl based solutions were not considered because of concerns about corrosion near contact. Table 1 summarizes the process splits and corresponding wafer identification. The aged solution was produced by treating 20 wafers with patterned photo resist in a dedicated bath 20 times for 30 second dips. The different cleaning treatments were processed simultaneously in designated baths to satisfy requirement of close coupling to next process step. After the cleaning process, the wafers were completed through the remaining process, and then PCM and reliability test.

TREATMENT	Wafers
15% FRESH NH4OH	13, 8
2%-AGED-NH4OH	9,2
2%-FRESH-NH4OH	4,18
8% FRESH NH4OH	11,5
ASH-2%NH4OH	1,15,20
ASH-15%NH4OH	3,14,19
ACETIC ACID	17,10
DI	12,16
NO-CLN	6,7

Table 1: Experimental matrix

The PCM test was performed using Agilent DC parametric test system 4071A. Device level reliability testing was performed on HBT transistors with emitter areas of 56μm^2 using custom built reliability test systems at Skyworks.[4] The transistors were subjected to high temperature and high current stress. The stress condition was 25KA/cm^2 emitter current density and 200^{o}C case temperature (~305^{o}C junction temperature). The electrical/thermal stress was interrupted periodically to allow device characterization to be performed at room temperature. A 50% DC current gain (beta) decrease was used as the device failure criterion. I-V curves of different BC diodes with varying area and perimeter were measured using Agilent 4155B semiconductor parametric analyzer.

RESULTS AND DISCUSSIONS

Figures 1, 2 and 3 show the BC diode turn on voltages, ideality factors and saturation currents measured, at PCM, for all wafers. The variants that had acetic acid clean, DI water clean, and no clean have distinctly lower BC diode turn-on voltage, higher ideality factor and saturation current compared to the other splits.

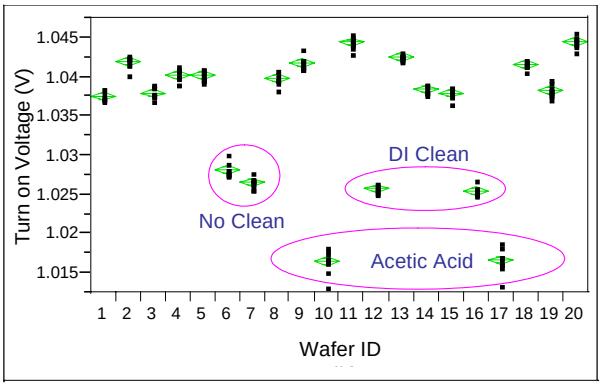

Fig 1: BC diode turn on voltage comparison

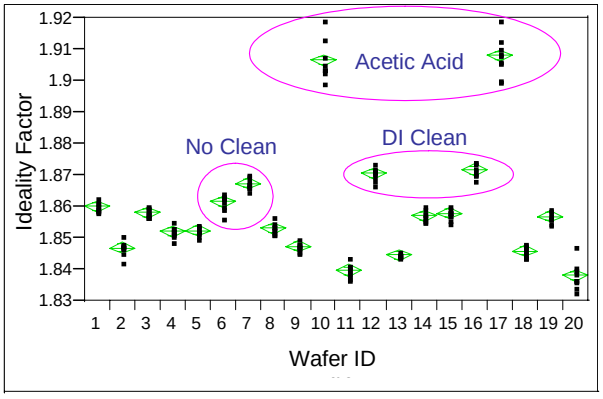

Fig 2: BC diode ideality factor comparison

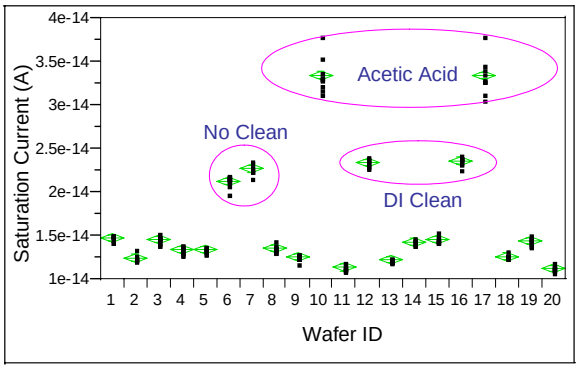

Fig 3: BC diode saturation current comparison

To further explore the differences in these important diode parameters, full I-V curves were measured. Figure 4 compares the I-V curves of a good diode, from the wafer processed with NH_4OH clean, and a bad diode, processed with no clean. For the bad diode, we observe a systematically higher current, for a given voltage, compared to a good diode. This indicates a poor choice in cleaning treatment leads to additional recombination current for a bad diode.

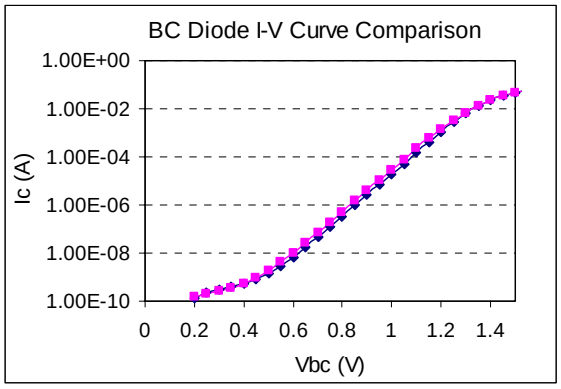

Figure 4: Comparison between the I-V curves of a good diode and an abnormal diode. The purple one is measured from the wafer processed with no clean and the blue one is from the wafer with NH4OH cleaning.

Subsequent reliability testing on HBT transistors shows that wafers with acetic acid clean, DI water clean and no clean also exhibit shorter stress lifetime. The transistors from these wafers start to fail (more than 50% drop in DC current gain) after approximately 100 hours of electrical and thermal stress, compared to 600-700 hours for NH_4OH cleaned wafers. This difference is shown in the probability plot of the transistor stress lifetime for these DOE wafers (Figure 5).

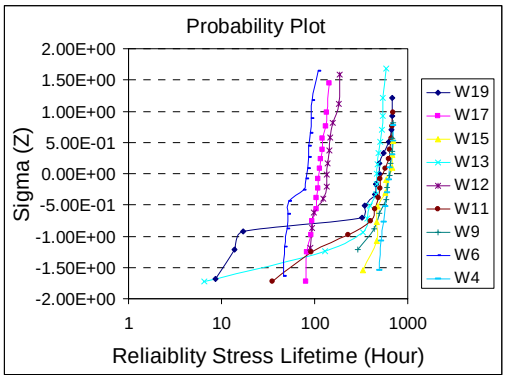

Figure 5: Probability plot of the transistor reliability stress lifetime. W6 (blue), W12 (brown) and W17 (purple) that are processed with no clean, DI water clean and acetic acid clean have short stress lifetime of about 100 hours.

The failure mode of the transistors with shorter stress lifetime is classical beta degradation characterized by the increase in base current (Figure 6). The BC diodes for these transistors were stable over the reliability stress (Figure 7), even though they have lower 0 hour turn on voltage compared to the good wafers.

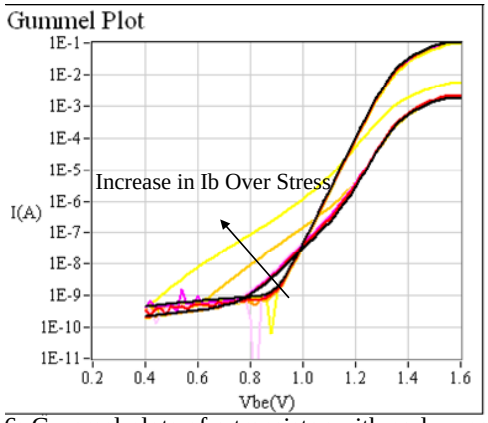

Figure 6: Gummel plots of a transistor with early wear out failure over reliability stress

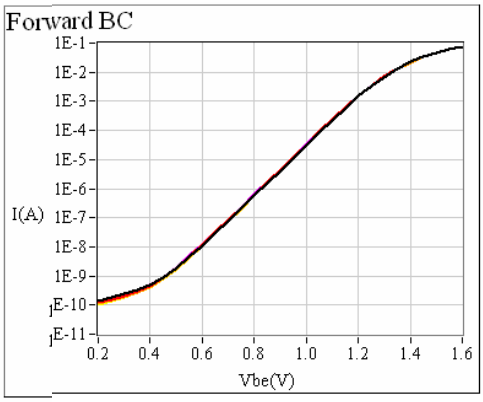

Figure 7: Stable I-V of the BC diode with lower turn on voltage over reliability stress.

It is well known that the passivation ledge has large impact on GaAs HBT characteristics.[5,6] Improper design and process can lead to device performance degradation and reliability failure. The surface cleaning process investigated in this work occurs after the base pedestal formation. The ledge surface and base pedestal sidewall are exposed to the cleaning solution. The fact that the wafers went through acetic acid clean, DI water clean, and no clean all have device performance shift (BC turn-on) and shorter lifetime indicates that the ledge and surface characteristics might be adversely affected by these cleaning methods.

Prior publication [1] shows GaAs surfaces treated with NH_4OH solution have less contaminants (such as C, O, N, S, and Cl) and nearly stoichiometric (i.e. equal Ga and As concentrations), compared to surfaces treated with HCl solutions. The work presented here confirms with this finding. The current work also shows that NH_4OH based cleaning solutions, either fresh or aged, various concentrations and with or without plasma ash, all result in acceptable surface characteristics and, in turn, device performance and reliability. As a result, NH_4OH cleaning provides good process margin. DI water clean, no clean, and acetic acid clean result in higher surface recombination current – lowering the diode turn-on voltage and long term reliability of the HBT. This is most likely caused by the inability of these cleans to sufficiently remove oxide layers or contaminants on the surface, or the formation of a reactive As rich surface.

Further work, using the limited number of available devices, was carried out to identify where the extra recombination current is located: base pedestal sidewall, and/or the ledge surface. We performed measurement on diodes with eight different sizes and geometries. The saturation current was extracted and further decoupled into base perimeter (P) and area (A) components: $Is=A*Is_A + P* Is_P$, where Is_A and Is_P are the respective saturation currents. By rearranging the equation, Is_P can be extracted by fitting the Is/A vs. P/A curve where Is_P is the slope of the line.

Figure 8 shows the Is/A vs. P/A plots for wafers processed with different cleaning methods. Even though some of the plots have large spread as evidenced by not close to unity regression coefficient (R^2), the wafers with no clean, DI clean and acetic acid clean generally have higher Is_P than that of the wafers with NH_4OH based cleaning. This indicates that the increased current may be due to periphery. However, due to the limited number of available structures, we were unable to further decouple the periphery recombination current as it could be either from the base pedestal sidewall or from the periphery of the leftover ledge near the base contact.

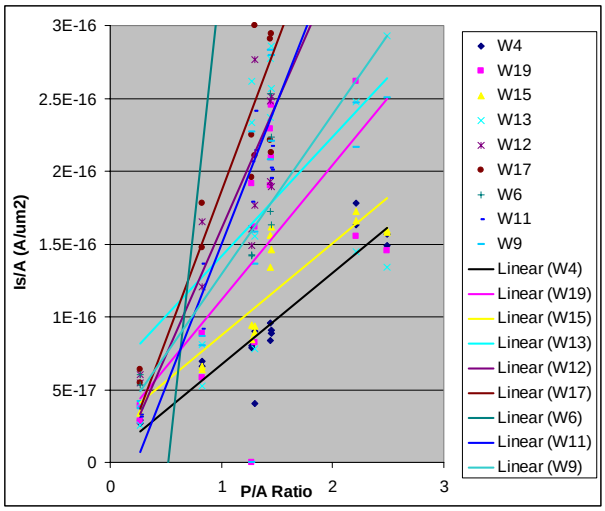

Figure 8: Plot of saturation current vs. periphery over area ratio.

FIB cross sections were taken on the transistors with early wear out failure in an attempt to identify any physical evidence of surface or structural deterioration that might be caused by the improper surface cleaning. However, there was no visible sign of defects, possibly due to the limited resolution with SEM. TEM analysis is needed as it has much higher resolution and can be more revealing for subtle surface/interface irregularity.

CONCLUSION

The results of this work indicate that NH_4OH based solution is a good choice for surface cleaning and processing of GaAs based HBTs since it results in high quality devices and has excellent process margin. The use of other cleaning procedures (no clean, DI water clean or acetic acid clean) leads to higher leakage currents and can result in significantly worse long-term device reliability. Our observations are consistent with previous work that indicates an NH_4OH solution produces a cleaner and more stoichiometric GaAs surface resulting in superior device performance.

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ACRONYMS

GaAs: Gallium Arsenide
HBT: Heterojunction Bipolar Transistor
PCM: Process Control Monitor
I-V: Current-Voltage
FIB: Focused Ion Beam
SEM: Scanning Electron Microscopy
TEM: Transmission Electron Microscopy