GaN on SOD Substrates – The Next Step in Thermal Control

J. Zimmer and G. Chandler

sp[3] Diamond Technologies Inc., Santa Clara, CA, jzimmer@sp3inc.com, gchandler@sp3inc.com

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Abstract

Compound semiconductor devices face severe thermal control problems as a result of increasing power densities which result from the need for more power and the ongoing reduction in geometries of individual devices. The solution to this problem is to place a heat spreader material as close to the device junction area as possible. For GaN devices this can be accomplished by growing a GaN device layer on top of a silicon on diamond (SOD) substrate where the silicon layer is thin and the diamond layer acts as a heat spreader that is within a few microns of the heat producing area on the device. This paper will discuss both the structure and performance advantages of GaN on SOD as well as some of the issues that will drive scaling and manufacturability from substrate fabrication through device packaging.

INTRODUCTION

Today's compound semiconductor industry faces significant challenges in heat management due to the impact of increasing power levels resulting from device density increases coupled with power increases in RF power devices and similar output energy increases in high luminance LED's and laser diodes. Both of these lead to increasing thermal loads on packages which do not have adequate thermal pathways for removing the heat. Historically, devices have been mounted into packages using soft or hard solders and packages were attached to heat sinks using thermal grease as an interface material. The resulting thermal path included both the full thickness of the die as well as the other components just discussed. Newer technologies use thinner die, higher heat conductivity substrates and more efficient packaging materials but junction temperatures are still climbing as chip power is pushed to higher and higher limits.

An additional problem is that heat is not generated uniformly on the chip so some locations are significantly hotter than others. This is true for most devices in the compound semiconductor world such as RF power devices, high brightness LED's, VCSEL's and traditional laser diode arrays. The current solution to this problem is to attach the device directly to a heat spreader so that heat is distributed across the entire area of the chip rather than being localized to specific areas. Unfortunately this still requires the heat to be extracted through the entire thickness of the chip prior to reaching either a heat spreader or a heat sink so the possibility of localized hot spots is still present.

The solution for all of these problems is to place the heat spreader as close to the heat generating areas as is physically possible. If this heat spreader layer is constructed of a CVD diamond layer and located within a micron or two of the active device then the device generated heat only has to move a few microns before it is spread across the entire area of the chip. The net result is to reduce both the local junction temperature as well as the overall chip temperature since the heat flow path is now the full area of the chip itself.

DISCUSSION

A structure of this type can be achieved by fabricating the compound semiconductor device layers such as GaN on SOD (silicon on diamond) wafers where the diamond heat spreading layer is only microns from the heat producing areas. The SOD substrate is fabricated using standard CVD diamond growth coupled with wafer bonding and polishing technology common in the silicon semiconductor technology world. The resulting substrate is a layered structure consisting of a thin single crystal silicon layer on top of a heat spreading diamond layer with a silicon handle wafer supporting that structure. Once the SOD substrate is fabricated then GaN device layers can be grown on the silicon layer using standard MBE or MOCVD processes. SOD substrates can be fabricated in sizes as large as 300 mm diameter and GaN MOCVD systems can be scaled at least to 200 mm diameters so the resulting structure not only provides optimum thermal properties but also allows process scaling to reduce volume manufacturing costs. Figure 1 shows a comparison of standard GaN and GaN on SOD technology for RF power devices.

SOD wafers as diagrammed in Figure 1 are equivalent to SOI wafers commonly used in the silicon semiconductor industry but the insulator (I) in an SOD wafer is diamond rather than silicon dioxide. The top layer of silicon is a micron or two thick and the diamond layer is several microns to tens of microns thick depending on the specific application. The underlying substrate is a full thickness silicon wafer which serves as a handle for processing and can be either thinned or completely removed prior to packaging. Diamond at this thickness has a thermal conductivity that is 2-3 times greater than copper and 10 times greater than silicon. This high thermal conductivity means that several microns of diamond can effectively

equalize temperatures across an entire chip at the device junction level. Local power densities of hundreds to thousands of watts per square mm are spread quickly over the total area of the chip and reduced to a few hundred watts per square centimeter at most. Heat flux at this level can be handled much more easily by initial die attach layers and subsequent heat spreaders and heat sinks as shown in Figure 2.

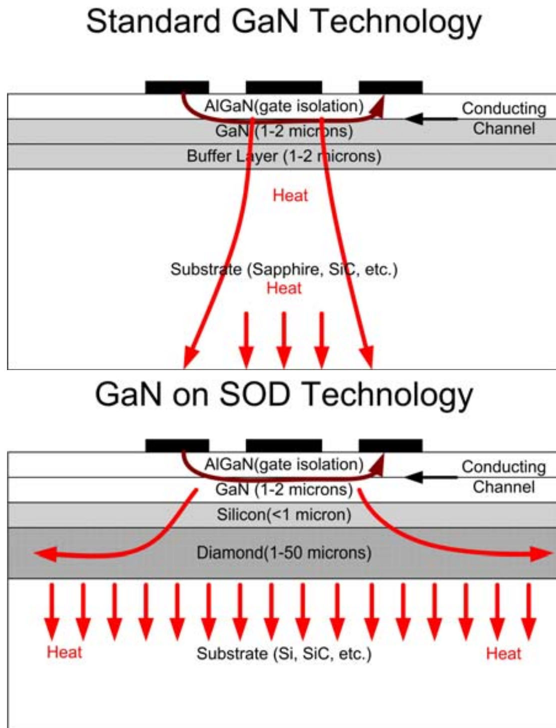

Figure 1
Standard GaN on silicon and GaN on SOD

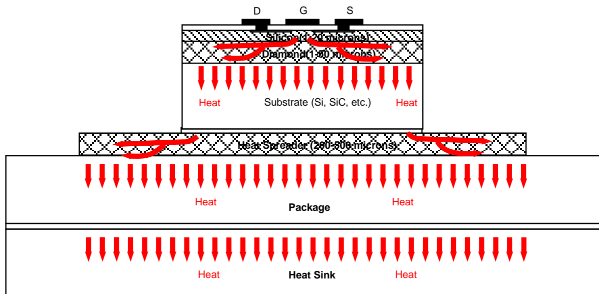

Figure 2
Heat flux in ideal packaged SOD device

The limit of this technology is determined by the ability of the solders, TIM layers, package materials and heat sinks to remove heat from the diamond layer. Under actual measured conditions, power densities as high as 1000 W/cm2 with junction temperatures below 120C have been shown to be possible on silicon devices on SOD substrates. This compares to 200 W/cm2 for equivalent thicknesses of silicon substrates. The results come from work done at NCSU by Dr. Sitar [1] as shown in Figure 3.

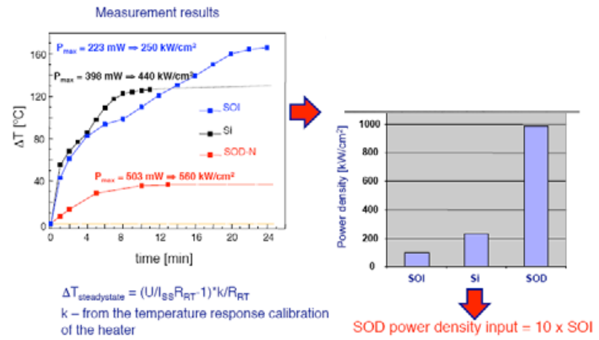

Figure 3
Measured Tj and performance as a function of substrate type

Comparable results can be obtained with GaN devices as well. The high frequency RF power device market is beginning to use GaN HEMT transistors where the GaN device layer is grown on either SiC or silicon substrates. Both of these can be replaced with SOD substrates with substantial improvements in device performance and/or reduced junction temperatures. Figure 4 is modeling work done by TriQuint Semiconductor and shows that for a constant junction temperature and three different diamond configurations the power level can be increased by more than 50% compared to GaN on SiC and more than 100% for GaN on silicon.

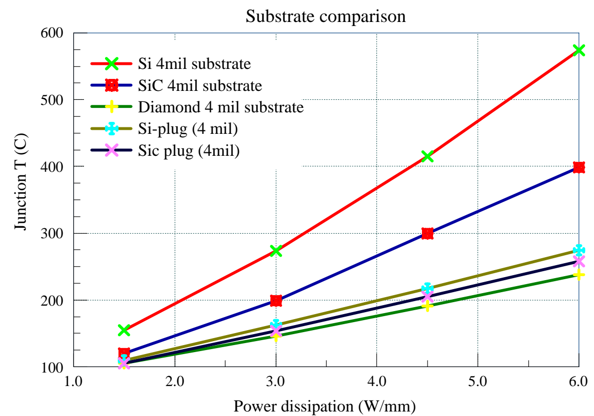

Figure 4
GaN device performance on various substrates [2]

Figure 5 shows the potential for junction temperature reduction as a means for improving device reliability. This modeling work done by Nitronex Corp. compares a commercial GaN on silicon power transistor with a comparable device built on an SOD substrate. The 40-50 degree junction temperature reduction can substantially improve long term device reliability.

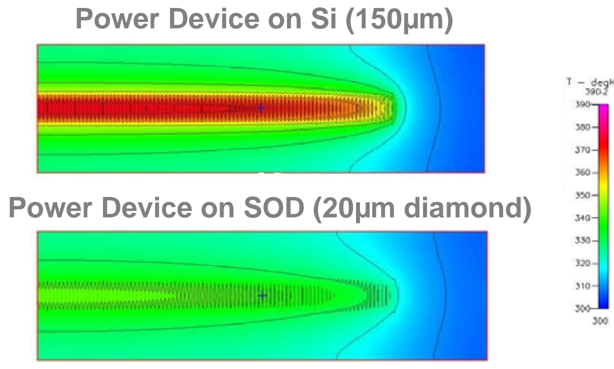

Figure 5
Junction Temperature Reductions with GaN on SOD [3]

For the growing white light illumination market this means that power levels can be increased substantially for both surface emitting LED's as well as vertical cavity surface emitting laser diodes (VCSEL's). Both can be made on GaN on SOD substrates which allow much higher power densities and luminosity than standard products.

Commercial fabrication of GaN on SOD substrates is not without its challenges however. Diamond has a substantial mismatch in the coefficient of thermal expansion when compared to silicon and GaN so the stress in the diamond and between the various layers must be balanced such that the final die is flat enough to go through a standard packaging cycle. In addition it must be flat during the SOD substrate fabrication process, flat during the GaN growth at >1000C and flat during the wafer processing steps after GaN growth and before thinning and segmentation. All of these steps require bow and warp of less than 100 microns TIR and some steps such as E beam lithography may require less than 25 microns across 100-200 mm of wafer diameter. Achieving these values requires that the substrate be engineered for neutral stress at each step in the overall lifecycle. Stress balancing layers applied or removed at various stages of the wafer lifecycle and also very uniformly distributed controlled stress in the diamond film itself must be maintained to achieve these goals. Figure 6 shows a typical substrate lifecycle where the substrate was engineered for flatness during wafer processing but without stress balancing layers. The result is a finished device die that has significant bow and cannot be packaged. Figure 7 shows the results of proper stress balancing where the substrate is flat throughout all of the critical processing steps and the finished die is also flat.

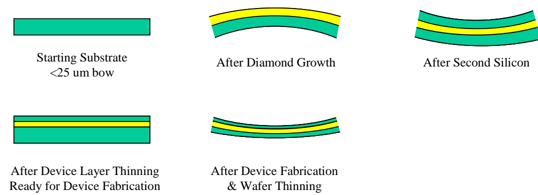

Figure 6
Uncontrolled wafer stress

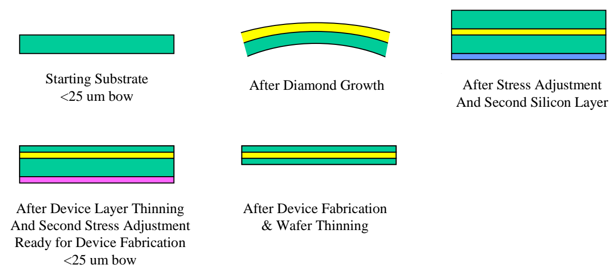

Figure 7
Controlled wafer stress

Assuming that the wafer stress is controlled properly, the GaN layer must be of sufficient quality to make devices. Figure 8 shows a plot of GaN device layer compositional uniformity from a layer grown on an SOD silicon device layer. Figure 9 shows a CV plot of the same device layer. Both of these plots demonstrate that device quality films can be grown successfully on the finished SOD substrates.

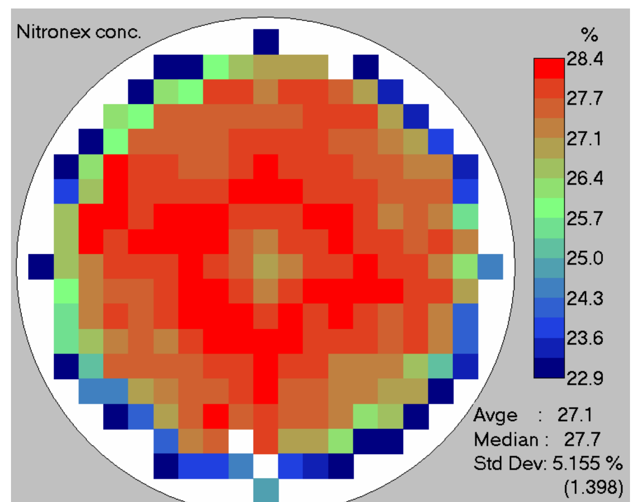

Figure 8
Compositional Uniformity Plot
AlN % in Device Layer

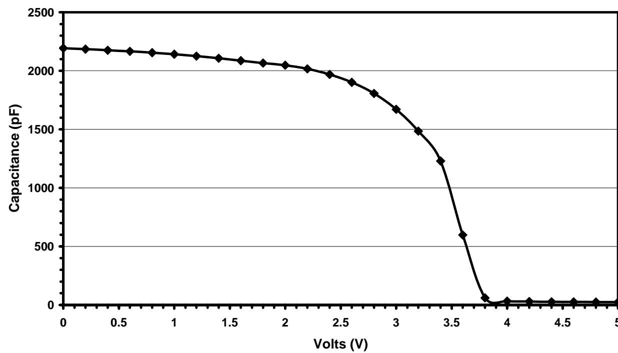

Figure 9
GaN Device Layer CV Plot

CONCLUSIONS

GaN on SOD substrates provide a path for increasing both power dissipation and reliability on a variety of compound semiconductor devices including power RF, power switching, high luminance LED's and VCSEL laser diodes. All of these products are possible and will evolve over the next decade from concept to mainline production if high performance wireless devices and solid state lighting evolve as expected in the compound semiconductor world. Each substrate will be customized to the application to optimize the thermal performance so the substrate variations will be as broad as the product application areas. Eventually all high performance high efficiency semiconductor devices will require the use of a heat spreading material such as diamond as close to the junction as is possible.

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[3] E. Piner, J. Roberts, Nitronex Corp., private communication

ACRONYMS

SOD: Silicon On Diamond
SOI: Silicon On Insulator
VCSEL: Vertical Cavity Surface Emitting Laser
TIM: Thermal Interface Material