

# High Yield Intra-Cavity Interconnection Fabrication Method And Characterization Methodologies

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## ABSTRACT

Northrop Grumman Space Technology has demonstrated the capability to manufacture intra-cavity interconnections (ICICs), which consistently yield greater than 99%. These ICICs are an integral part of MMICs packaged at the wafer level using wafer bonding techniques. Efficient test structures were designed to evaluate these interconnects, allowing fast on-wafer assessment of interconnect yield in a production environment.

## INTRODUCTION

Northrop Grumman Space Technology has developed a low-temperature wafer-level packaging (WLP) technology [1-5], that, to our knowledge, is the first MMIC-compatible hermetic packaging process suitable for batch fabrication of high-performance, radio-frequency (RF) MMICs. This WLP technology enables 3-D heterogeneous integration of high-performance RF circuits which are typically fabricated on dissimilar substrates. Three-dimensional interconnection within the WLP package is an essential part of heterogeneous integration. These 3-D intra-cavity interconnections (ICICs) can greatly reduce losses associated with signal routing between different circuits or functional blocks by eliminating unnecessary wire-bonding between chips and by decreasing overall routing distances. Low loss, compact ICICs can significantly enhance circuit performance by reducing parasitics in signal routing, enhancing circuit speed, and enabling new circuit architectures.

## WAFER-LEVEL PACKAGING TECHNOLOGY

NGST's low temperature WLP technology is utilized to fabricate the intra-cavity interconnections (ICICs). The ICICs and the hermetic sealing of the packages are formed simultaneously during the wafer bonding process. A brief introduction to NGST WLP is presented here.

The WLP process developed at Northrop Grumman is a batch fabrication that is applied after the standard MMIC

processes. As a result, MMIC performance is not compromised during packaging. This preserves the existing high-reliability production process controls already in place. This packaging process combines the benefits of solder bonding and metal alloy bonding, maintaining the desired characteristics of low temperature solder bonding and thermodynamically stable alloy bonding. It is highly topology tolerant, producing high bonding and interconnection yields while maintaining low bonding temperature. It enables bonding of a multiple wafer stack and is compatible with standard assembly processes such as solder bumping. The bonding temperature does not exceed 180°C, resulting in very low built-in stress, thereby making it suitable for packaging high performance RF MMICs and for multi-wafer heterogeneous integration.

NGST's baseline WLP is a two-wafer process that consists of a substrate and a cover wafer. Figure 1 shows the simplified flow of the WLP processes. The substrate and cover halves are first processed separately using standard MMIC batch fabrication processes. Matching metallic bonding rings are deposited on the two wafer halves at the end of the front side processes. Fabrication of the individual wafers is completed through the backside processes before wafer bonding is performed. The two completed wafers are then aligned using a wafer aligner. The aligned wafers are then bonded using a permanent wafer bonder that applies force to the wafers while simultaneously heating the top and

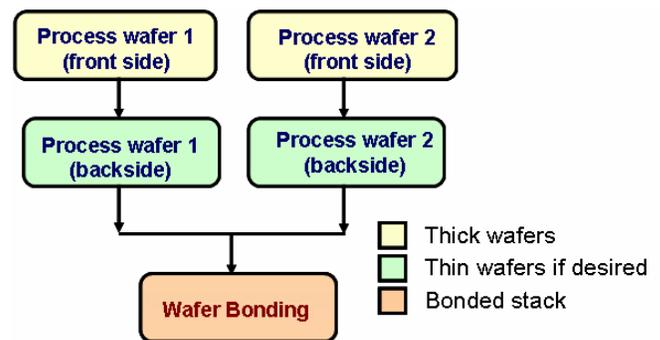
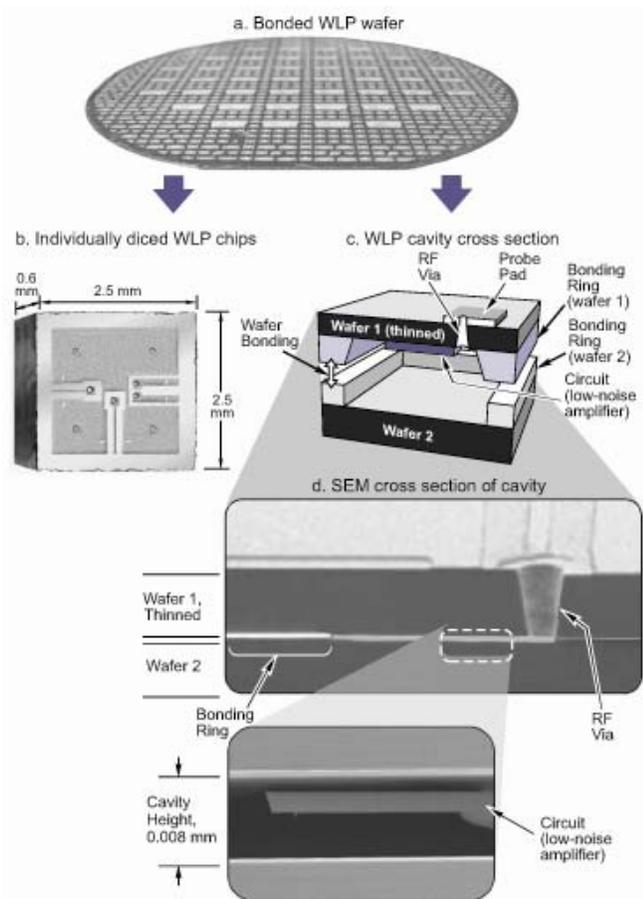


Figure 1. Simplified WLP process flow.



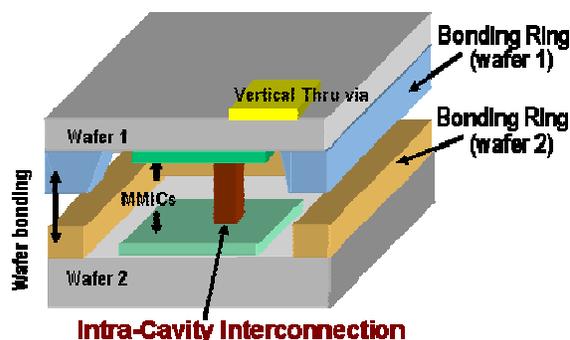
**Figure 2:** (a) A bonded wafer pair, (b) an individually diced package, (c) Illustration of a WLP cavity cross-section, (d) SEM of a WLP cross-section.

bottom wafers. This low-temperature wafer-level bonding process fuses the sealing rings of the two wafers together. The cavities are created between the two wafer halves, encapsulating the front side of the circuits within the cavities at the wafer level. A bonded wafer pair and cross section of a WLP cavity are shown in Figure 2.

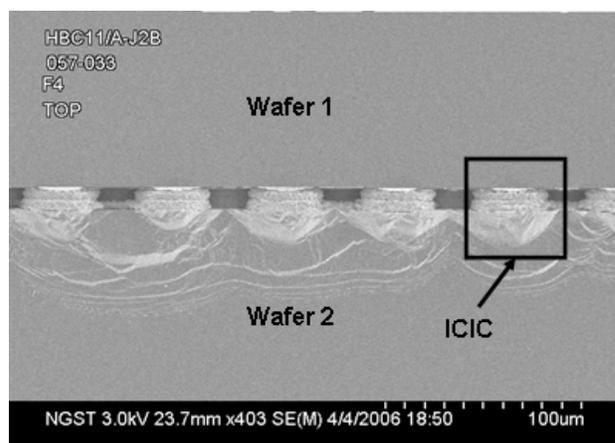
WLP devices are processed using batch fabrication at the wafer level. They can be diced into individual chips, using conventional techniques to saw through the wafer stack. Figure 2a is a photograph of a bonded WLP wafer. These particular individually diced WLP chips (Figure 2b) are  $2.5 \times 2.5$  mm in chip dimension, and only 0.6 mm thick. A cross section illustration of the WLP cavity is shown in Figure 3c, and the corresponding SEM micrograph is shown in Figure 2d. The cavity formed between the two wafers is only about 0.008 mm. In this configuration, the packaged MMIC circuits, shown upside down inside the cavity, are tested by accessing the probe pads on the back side of the package.

## INTRA-CAVITY INTERCONNECTIONS (ICICs)

The intra-cavity interconnections (ICICs) are formed between the two inner wafer surfaces inside the WLP cavity. An illustration of an ICIC inside the package is shown in Figure 3. The ICICs are patterned at the same time as the WLP bonding rings on both wafer halves, and therefore, no additional processing steps are required for ICIC formation. A SEM cross-section of an ICIC chain between two wafers is shown in Figure 4.



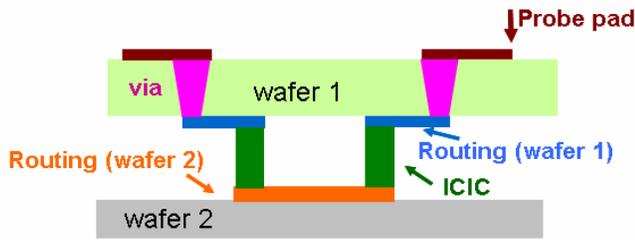
**Figure 3:** Illustration of an ICIC inside WLP.



**Figure 4:** SEM cross section of ICICs.

## INTERCONNECT TEST STRUCTURE

Test structures with various ICIC diameters, spacings, and chain lengths were designed and fabricated to evaluate ICIC yield. All of the test structures are designed with a standard 8-probe pad to be compatible with NGST's automated on-wafer testing for fabrication monitoring purposes. Schematic cross-section of a 2-ICIC daisy chain, shown in Figure 5, consists of both vias and ICICs. Kelvin structures and via test structures were incorporated in the test structure to measure ICIC connections as well as functionality of the vias that are in series with the ICICs. The individual ICIC and via yields are calculated from structure yield by using binomial methods: Individual



**Figure 5:** Schematic cross-section of a yield test structure.

Yield = (structure yield)<sup>(1/number of interconnects)</sup>. Test results are discussed in the next section.

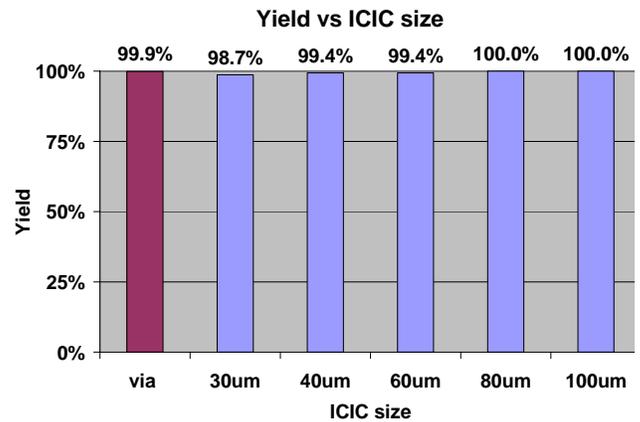
### TEST RESULTS

A number of the ICIC test structures, shown in Figure 5, were implemented to evaluate the impact of ICIC diameter on yield. Data is shown in Figure 6. This data is obtained by the binominal formula provided above, where the number of interconnect/via is 2. Via yield is greater than 99.9%, and greater than 99% interconnect yields were obtained from ICICs with diameters greater than 30um. This particular data is obtained from wafer pairs consists of two GaAs substrates thinned to 4mils. The same experiments were repeated with different wafer thickness combinations to study the effect of wafer thickness on ICIC yield: Wafer combinations with 2mil GaAs (wafer 1) bonded to 4mil GaAs (wafer2), 4mil GaAs (wafer 1) bonded to 25mil GaAs (wafer 2), 2mil GaAs (wafer 1) bonded to 25mil GaAs (wafer 2) were evaluated. Similar yield numbers were obtained and we found that wafer thickness is not a factor effecting ICIC yield. ICICs with 30um diameters exhibit a yield of ~99%, slightly less than others.

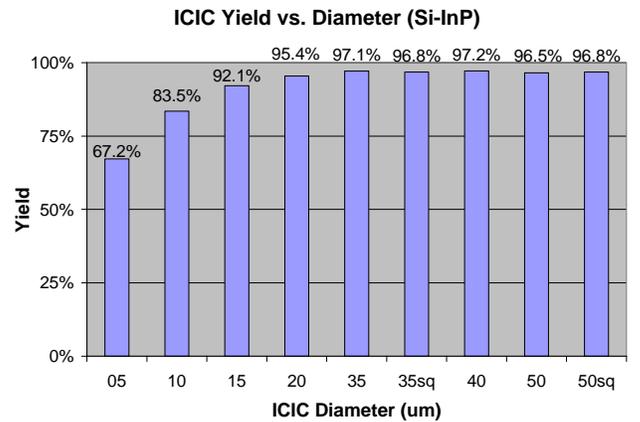
To further understand yield limitations with respect to ICIC diameters, we designed structures with ICIC diameters down to 5um. Data summary shown in Figure 7 is obtained from wafer pairs consist of 3mil InP wafers bonded to 25mil silicon wafers. Greater than 67% yield was obtained from ICIC diameters of only 5um. We suspect that the yield loss observed from smaller ICIC diameters is due to the alloy volume unable to overcome local cavity height variance. We are currently investigating this theory by adjusting bonding force parameters to overcome cavity height variance and by increasing alloy volume to enhance ICIC's ability to overcome local topologies.

### CONCLUSIONS

Northrop Grumman Space Technology has developed a technology that is capable of producing high yield Intra-Cavity Interconnects (ICICs). These interconnections provide signal routing between circuits residing on the facing surfaces within a sealed package. They are fabricated by batch processes and are fully compatible with NGST's MMIC production processes. Greater than 99%



**Figure 6:** ICIC & via yield data obtained from GaAs wafer pairs (4mil GaAs + 4mil GaAs).



**Figure 7:** ICIC & via yield data obtained from InP-Si wafer pairs (3mil InP + 25mil Si).

interconnection yield is consistently obtained from wafer pairs with different substrate thickness and substrate materials. NGST has developed a robust, high yield interconnect process which enables 3D heterogeneous integration of MMICs.

### ACKNOWLEDGEMENTS

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