Gain Enhancement of Junction PHEMT Power Amplifiers for Cellular Phones

Kazuki Nomoto, Koichi Hirata, and Mitsuhiro Nakamura

MMIC Development Section, LSI Device Engineering Department, Sony Semiconductor Kyushu Corporation,
Kagoshima Technology Center, 5-1, Kokubu Noguchi-kita, Kirishima-shi, Kagoshima, 899-4393 Japan
E-mail: Kazuki.Nomoto@jp.sony.com, Phone: +81-995-47-3739

Abstract

In this paper, we report a significant gain enhancement of junction pseudomorphic high electron mobility transistors (JPHEMTs) for wideband code division multiple access (W-CDMA) power amplifiers (PAs). By employing a novel device design characterized by a gate-drain recessed structure, gate gold plating, and optimized device parameters such as doping concentration and barrier layer thickness in the epitaxial structure, a 3.0 dB gain enhancement was achieved with 52 % power added efficiency (PAE) at a 17.2 dBm output power (P_{out}), a -40 dBc adjacent channel leakage power ratio (ACPR), and a supply voltage of 3.5 V in a 1.95 GHz W-CDMA class-AB operation. This novel device was developed by making changes and improvements to our existing mass production technology, the Microwave Monolithic Integrated Circuit (MMIC) process.

INTRODUCTION

High efficiency, low distortion, and high gain are the most important performance indicators for handset PAs due to increasing demands for longer talk-time and device miniaturization. To meet these demands, we have been developing a high efficiency PA device design using JPHEMTs with pn junction gates [1, 2]. Due to their unique gate structure, these devices exhibit excellent characteristics such as a low on resistance (R_{on}) of 1.1 ohm mm and a high gate voltage of 1.3 volts at a 1mm gate width. A two-stage PA design substantially contributes to miniaturization. However, practical application was thought to be difficult because our original device had inadequate gain characteristics for systems, such as W-CDMA and UMTS, that require a high output power of 27.5 dBm and above. A high gain PA with at least 2.0 dB of gain improvement has been considered absolutely essential for such systems.

In this paper, we report a 3.0 dB gain enhancement in a JPHEMT PA under conditions of W-CDMA modulation at 1.95 GHz. This result was achieved by employing a novel gate-drain recessed structure, optimized doping concentration and gate gold plating as techniques for reducing gate-drain capacitance (C_{gd}) and gate resistance (R_g).

DEVICE DESIGN

To support our efforts at enhancing PA device gain characteristics, we employed two simulators for improving device structure. Small-signal equivalent circuit simulation results, depicted in Fig. 1, indicated that C_{gd} reduction would improve small-signal frequency characteristics and that reduction of R_g would further improve f_{max} frequency characteristics.
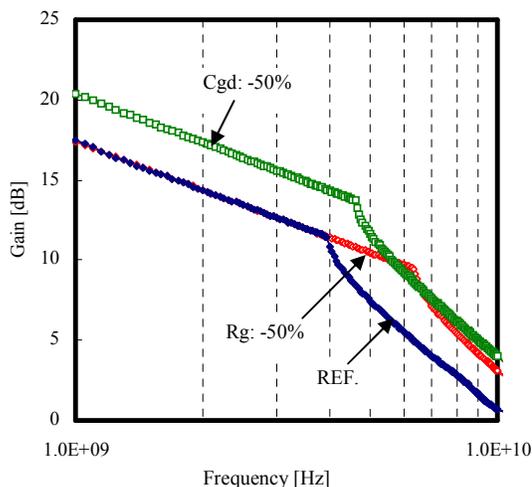

Fig. 1   Simulation of small-signal gain.

While it is widely reported that field plate technologies can be employed for high power applications such as base station power amplifiers to reduce C_{gd} and improve breakdown voltage [3, 4], we chose a local recessed technology, which was designed for use between the gate and drain of JPHEMTs to reduce feedback capacitance by carrier reduction. In this study, several recession depths were examined for optimization with respect to DC and RF characteristics. In addition, since simulation results indicated that doping concentration reduction in the epitaxial structure and barrier layer thinning could also be attributed to C_{gd} decrease, we also examined various doping concentration devices for both DC and RF characteristics.

We simply describe the epitaxial structure in this study. Following growth of an AlGaAs/GaAs multiple buffer layer on a semi-insulated GaAs substrate, an n-AlGaAs doping layer, an undoped AlGaAs lower spacer layer, an undoped InGaAs channel layer, an undoped AlGaAs upper spacer layer, n^+-AlGaAs doping layer and n^--AlGaAs layer were sequentially fabricated.

Based on device simulation results, gold plating was applied to the gate to achieve R_g reduction. Also based on simulation results as well as recessed depth controllability for manufacturing, barrier layer thickness was designed to be 25% thinner than that of the standard device. In addition, several devices with lower epitaxial structure doping concentrations than our standard device were examined for purposes of C_{gd} reduction. A concentration of 3.0×10^{18} cm^{-3} was set as a reference, and devices with 10%-20% lower doping concentrations were tried. Moreover, we used a novel device design characterized by a gate-drain recessed structure similar to the examined devices, all of which had varying recessed depths. Fig. 2 shows a cross sectional view of the new device structure. Starting with the standard device structure, the recessed region was successfully fabricated on a 6 inch GaAs substrate by extending the Reactive Ion Etching (RIE) process time of the SiN etching mask.
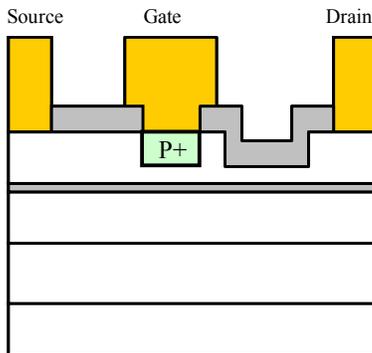

Fig. 2   Device structure.

RESULTS AND DISCUSSION

Cross sectional analysis

A typical cross sectional view of the new device was analyzed. According to results of cross sectional analysis, the gate gold plating and gate-drain recessed region were made with a high degree of precision in depth and width - with a target depth of 70 nm and target width of 400 nm - and in the placement of the recessed region. Meanwhile, the recessed region was designed to optimize width and position. The recessed region should be as narrow as possible to minimize carrier degradation and subsequent R_{on} deterioration. As for the recessed region's position, we have

confirmed that the closer it is to the gate, the more C_{gd} characteristics are optimized. With these two factors in mind, the recessed region was optimally fabricated to the extent possible within various process constraints such as those involved in photo lithography or etching.

DC Characteristics

As a part of our device characteristics investigation, we first measured DC characteristics. Three IV curves of examined devices with different doping concentrations are shown in Fig. 3 for non-recessed devices and Fig. 4 for recessed devices. IV curves of the examined devices indicate lower currents than that of the reference device, whose doping concentration was 3.0×10^{18} cm^{-3}, because a 10 % or 20 % doping concentration reduction and a gate-drain recession of 70 nm led to a carrier decrease in the channel. This can be seen clearly in the bold line for the two graphs. However, Fig. 3 and Fig. 4 indicate that the recessed structure has little effect on current decrease in the case of comparatively high doping concentrations of 2.7×10^{18} cm^{-3} or 3.0×10^{18} cm^{-3}.

Fig. 5 shows the relationship between doping concentration and R_{on} within the parameter of recessed depth. As shown in Fig. 5, R_{on} is inversely proportional to the doping concentration. As with IV characteristics, R_{on} begins to degrade considerably at a doping concentration of 2.4×10^{18} cm^{-3}. We considered the doping concentration-R_{on} relationship reasonable because R_{on} behavior was consistent with sheet resistance characteristics, which depend on carrier concentration, when calculated using the Transmission Line Method (TLM). While the final device design would be determined after observation of large-signal RF measurement, a device with a 20 % lower doping concentration was not expected to be practical from the standpoint of I_{ds} and R_{on} characteristics.
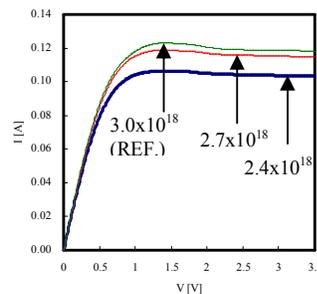

Fig. 3 $V_{ds} - I_{ds}$ (not recessed).
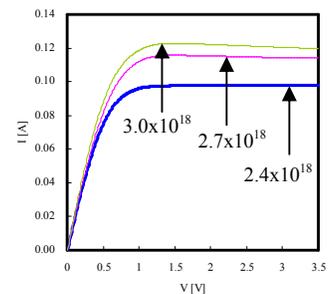

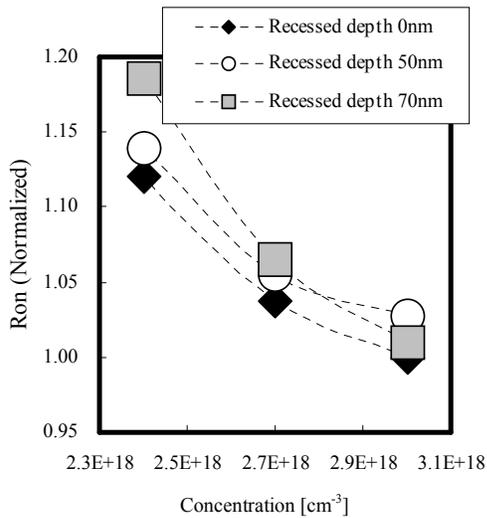Fig. 4 $V_{ds} - I_{ds}$ (recessed).

Fig. 5   Concentration dependence of R_{on}.

RF characteristics

Following the DC characteristics investigation, we measured small-signal characteristics for the examined devices within a frequency range of 0.1 to 20.1 GHz. Device parameters derived from Scattering-parameter (S-parameter) were monitored at 1.95 GHz. Fig. 6 shows S_{11} characteristics, which indicate the device's input side impedance mainly consisted of R_g. As shown in Fig. 6, gate gold plating reduced R_g considerably, by a factor of two. We confirmed that the f_{max} of the new device was improved, as our Fig. 1 simulation predicted.
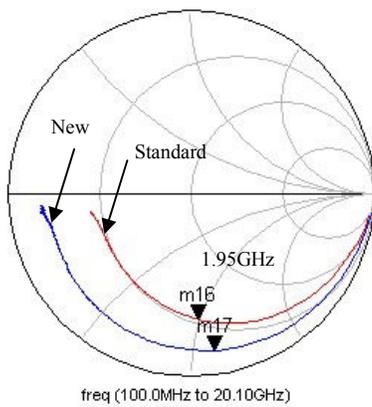

Fig. 6 S_{11}.

Doping concentration dependences of C_{gd} and MSG (Maximum Stable Gain) are shown in Fig. 7 and Fig. 8, respectively. As described in Fig. 1, C_{gd} reduction contributes to MSG improvement. We recognized that increasing recessed depth and reducing channel doping concentration were both very effective ways of reducing C_{gd}.

Based on the results shown in Fig. 7 and Fig. 8, we can see that the effects of a 50 nm depth recession and a 20% lower (than the reference) doping concentration are approximately equivalent with respect to C_{gd} reduction and subsequent MSG improvement. However, in view of DC characteristics such as I_{ds} and R_{on}, the possibility should be considered that device recession improves total device performance more effectively than doping concentration optimization.
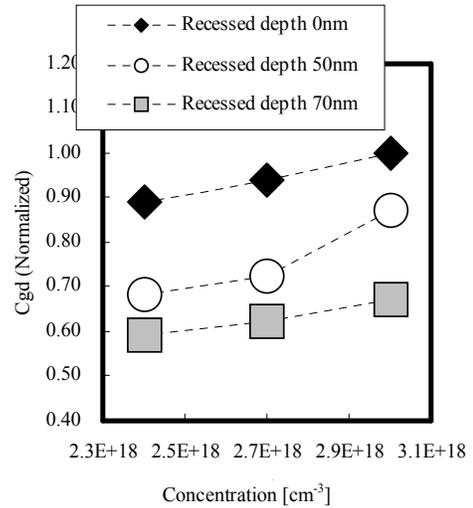

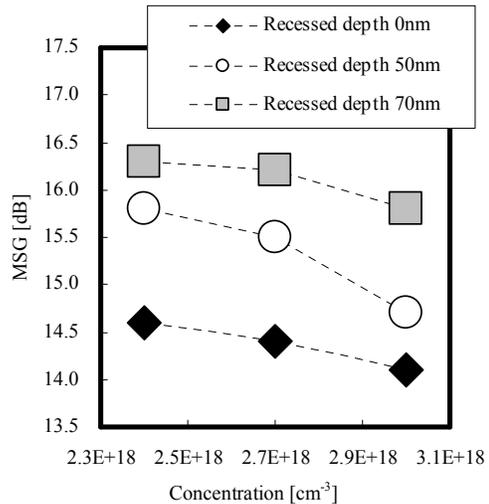
Fig. 7   Concentration dependence of C_{gd}.

Fig. 8   Concentration dependence of MSG.

Based on DC and RF measurement results, we chose a device with a doping concentration of 2.7×10^{18} cm^{-3} and a recessed depth of 50nm as a candidate for the new device design. Under conditions of P_{out} = 17.2 dBm, PAE = 52 %,

ACPRL1 = -40 dBc, our new device showed a 17.9 dB gain, which was about 3.0 dB higher than that of our conventional device. Fig. 9 shows a comparison of large-signal characteristics. We believe that this gain improvement can be attributed mainly to the reduction of R_g and C_{gd}. It is also important to note that PAE maximum improved about 2.5%. While not yet proven, the relationship of these improvements to C_{gd} reduction can be reasonably hypothesized.
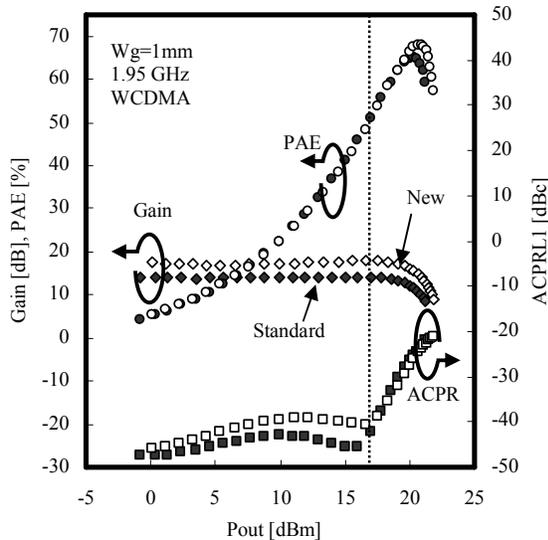

Fig. 9   Large-signal characteristics.

CONCLUSIONS

In this paper, a novel device structure characterized by gate-drain recession is investigated as a feedback capacitance reduction technology contributing to power amplifier gain enhancement for cellular phones. The device's design is distinct from field plate technologies recently reported. Gain properties of JPHEMTs for PAs were significantly enhanced by modifying our existing mass produced device's structure to employ gate gold plating for R_g reduction and gate-drain recession and lower doping concentration for C_{gd} reduction.

References
[1] N. Saka et al., IEEE GaAs IC Symposium Technical Digest, 301-304 (2003)

[2] M. Nakamura et al., IEEE MTT-S Digest, 1095-1098 (1999)

[3] Y. Ando et al., IEDM Technical Digest, 576-579 (2005)

[4] R. Therriien et al., IEDM Technical Digest, 568-571 (2005)

ACRONYMS
JPHEMT: Junction Pseudomorphic High Electron Mobility Transistor
W-CDMA: Wideband Code Division Multiple Access
PA: Power Amplifier
PAE: Power Added Efficiency
ACPR: Adjacent Channel leakage Power Ratio
MMIC: Microwave Monolithic Integrated Circuit
GaAs: Gallium Arsenide
SiN: Silicon Nitride
RIE: Reactive Ion Etching
TLM: Transmission Line Method
MSG: Maximum Stable Gain