Industrial GaInP/GaAs high Power HBT Process for S-Band and L-Band Applications

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Abstract

UMS have developed an industrial power HBT process especially dedicated to high power applications in L- and S-Band. Special care has been given to temperature management, required by the technology high power handling capability. Features include a thick thermal drain, for better temperature uniformity and stability, and passive elements for on-chip matching and stabilization circuit. Finally, the technology has been optimized for outstanding reliability as required for space, commercial and military applications.

INTRODUCTION

Despite the very large potential of wide-band gap devices and the significant progress made in the last years in terms of reliability, only very few commercial products are available that satisfy all potential customer requirements. This is especially true for very demanding military and space applications. There is therefore room for highly reliable GaAs-based power technologies to bridge the gap until sufficient WB-based products are available. We report here on the development and industrialization of a highly reliable power HBT technology. UMS have been involved in Power HBT technology since its foundation and has already successfully developed an X-Band power process for very demanding space and military applications [1, 2]. The technology being reported here is a further development featuring increased biasing voltage, improved thermal management, increased output power and operation up to S-Band.

EPITAXY

The process is based on commercially available GaInP-emitter structures. The collector and base layers doping and thickness have been chosen in order to guaranty base-collector and emitter-collector breakdown voltages in excess of 65 and 35 volts respectively. This is required to allow safe operation at a minimum of 20V collector bias. In particular, sufficient margin needs to be planned to take into account non-ideal matching and harmonic tuning as is typically being encountered in high performance wideband power applications. The emitter layers include an integrated ballast resistor to improve the thermal stability of the power devices.

FABRICATION PROCESS

The technology runs on our standard 4-inch fab using stepper lithography. Selective etching is extensively used in the fabrication process, resulting in excellent uniformity, and reproducibility of the critical parameters. This is especially important for the etching of the emitter, and can be controlled on the base sheet resistance measured on TLM modules. The non-alloyed emitter contact is based on a fully refractory metal that guarantees perfect stability and excellent reproducibility. Base and collector contacts are similar to the X-Band power process [1]. The transistors have a ledge passivation guaranteeing high current gain and excellent reliability. The device isolation is obtained through Boron implantation. Although the targeted applications do not call for fully integrated circuits, passive elements have been integrated to increase design flexibility. This is especially useful for very large power devices, where an on-chip pre-matching can significantly ease the HPA integration, and for effective oscillation cancellation. Finally, the power transistors feature a thick thermal drain, which allow for a maximum output power and an excellent thermal stability. The next section gives more details regarding the thermal drain.

TABLE I
KEY PARAMETERS OF UMS S-BAND POWER HBT TECHNOLOGY [a]

Symbol	Name	Value	Unit
R_sheet_B	Base sheet resistance	150	Ohm/sq.
BV_BC	Base-Collector breakdown	70	
BV_CE0	Emitter – Collector breakdown	36	V
Bmax_s1230	Maximum current gain	50	-
Re_S1230	Emitter resistance	12	Ohm
MSG_3	Maximum Stable Gain at 3GHz (20mA – 6V)	18	dB

[a] transistor parameters measured on a 2-30µm single-finger device

The process capability, including uniformity, reproducibility and yield, is being continuously monitored based on PCM results and on-wafer power bar characterization. Figure 1 shows the trend chart for base-collector and emitter-collector breakdown voltages demonstrating the very low fluctuation obtained on around 80

wafers. Figure 2 shows the corresponding distributions for over 1400 measurements points yielding a standard deviation of 4% for both parameters. When looking at individual wafers, the standard deviation drops to less than 2%. This is very close to the epitaxy homogeneity and illustrates the very good process uniformity.

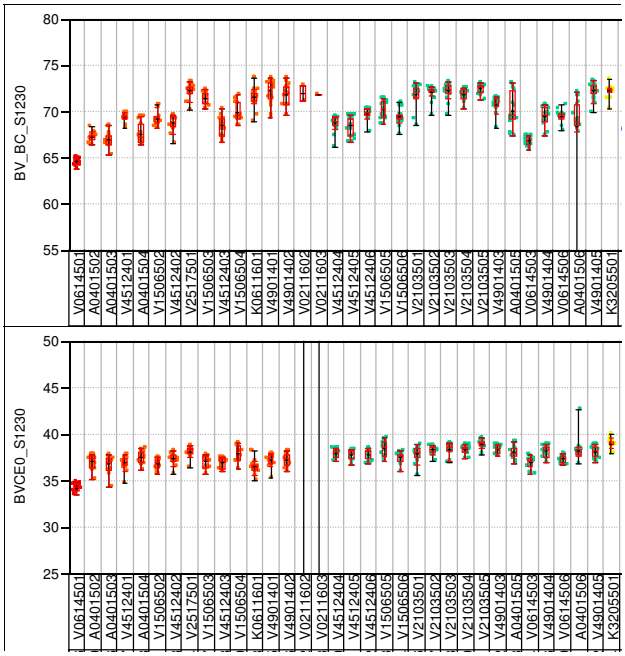

Figure 1: Trend-chart of base-collector (top) and emitter-collector (bottom) breakdown voltage (PCM - 2x30micron device).

POWER DEVICES

The major focus was placed on increasing the power cell dimensions and improving the thermal behavior to reach maximum output power and high frequency performances. The thermal optimization is essential and determines the best compromise between maximum power density and maximum temperature. Reliability and thermal run-away issues limit the later. The major step to reduce thermal resistance consisted in increasing the thermal drain thickness. Modifying the cell design can also help reduce Rth, for instance by increase the finger spacing, but with a negative impact on the high frequency performance. Varying thickness up to 35 µm were tested, but early experiments showed that the increased thickness could have a detrimental effect on reliability behavior. Analysis of the data showed a new failure footprint compared to those already known from our existing HBT technologies. Although it is difficult to bring an absolute proof, we believe that this new failure mechanism is linked to the increased mechanical stress generated by the thicker thermal drain. To investigate this effect further and optimize the cells we performed thermo-mechanical simulation. This allowed us to determine the weak points in the cells and helped us design new cells with optimum mechanical behavior.

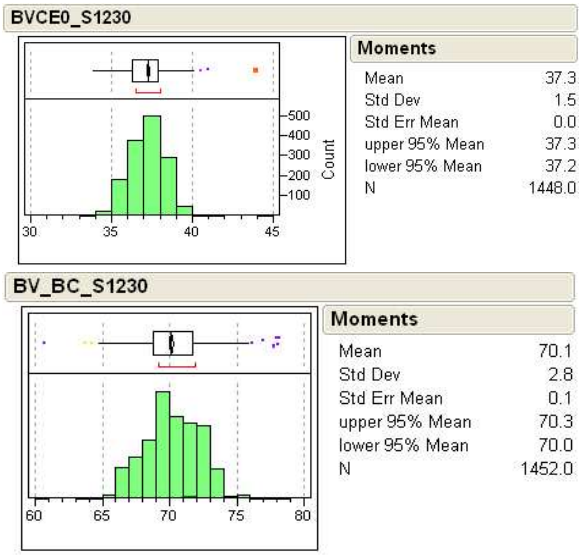

Figure 2: Distribution of BVce0 and BVbc0 for 1450 measurements accross 80 wafers.

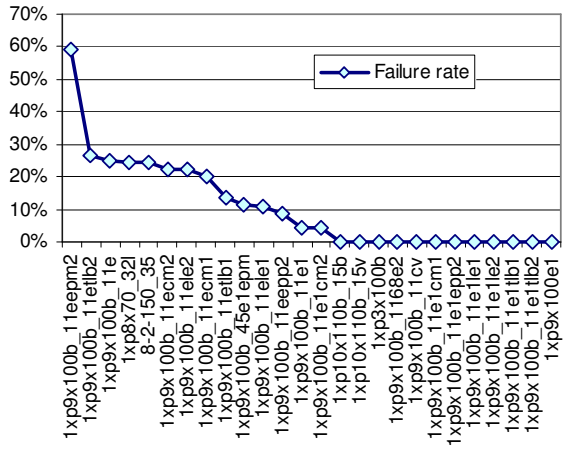

Figure 3: Failure rate after mechanical stress for various power cell designs.

In parallel, we designed a dedicated experiment to quickly test and compare the cells. The test is based around a temperature cycling procedure which conditions have been chosen to result in the worse possible mechanical stress seen by the devices in the applications. The behavior of the transistor is monitored through electrical characterization before and after the test. We found that not only the maximum temperature but also the ramp applied plays an important role in the test. Through this procedure it was finally possible to determine the best designs. Figure 3 shows the failure rates observed on various power cell designs. It is

clearly visible that the design has an important impact on the failure rate. These results were widely consistent with the thermo-mechanical simulations, which confirmed our assumption that the mechanical stability of the transistors was mainly responsible for the degraded reliability. However, the simulation alone would not have been sufficient to accurately quantify the effect and both experiments and simulation were finally necessary to select the most robust designs. After this first selection, the best candidates were then put through long-time aging test to validate their overall reliability performance.

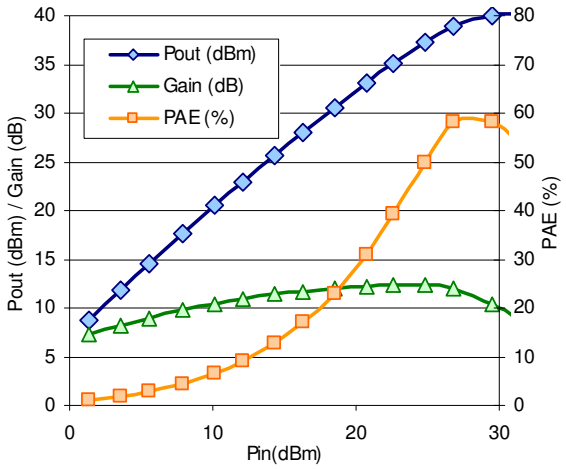

Figure 4: Power performance of a 1,800-µm emitter periphery transistor - f=3.1GHz - Vce=20V - B class.

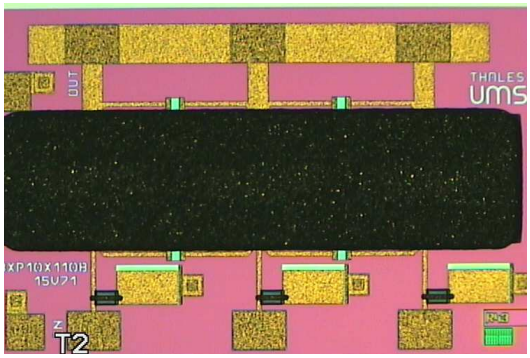

Figure 5: Picture of a 15-W power bar.

The obtained devices also demonstrated excellent high frequency power performances. Figure 4 shows the power performances obtained on a 1800-µm emitter periphery transistor at 3.2GHz. The output power reaches 10W, which corresponds to over 5W/mm. Note that at this operating point, and the associated power, the transistor supports high VSWR without electrical failure. Under optimum 50-ohm environment, such a power transistor reaches easily more than 8W/mm. Similar power cells can be combined on a chip to form so called power-bar to reach higher power levels (see Figure 5). Single power bar devices can be manufactured with excellent yield to deliver above 40W RF power [3, 4] and can be combined to achieve power levels above 100W. Figure 6 shows the collector current mapping of 35-W power bars measured on a 4-inch wafer. This demonstrates the excellent yield and uniformity obtained.

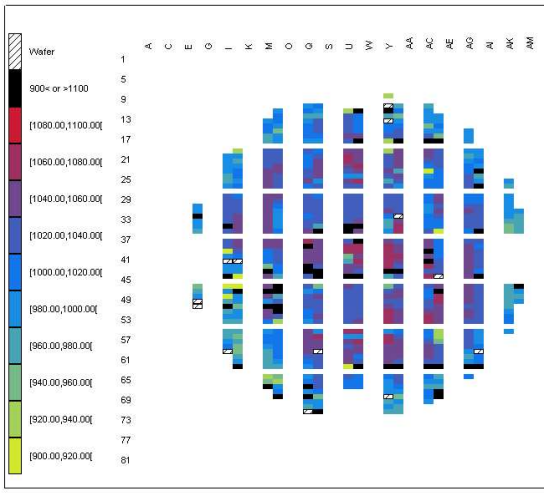

Figure 6: on-wafer mapping of the collector current at fixed base current (25mA) for 35W power bars. (716 devices tested). Mean = 950mA – std. Dev. = 33mA

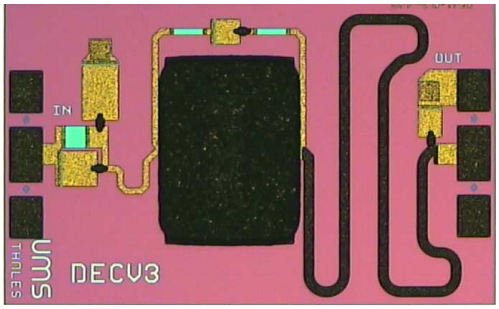

Figure 7: Photograph of a pre-matched power cell for reliability testing.

RELIABILITY

During the technology development, the transistors reliability has been permanently monitored, either through strongly accelerated on-wafer aging tests [5] or through long-time aging tests of large power cells. For the later, specific devices have been designed to guaranty an easy and stable testing on one hand and allow DC as well as RF (small- and large-signal) tests on the other hand. Figure 7 shows a picture of such a test device. As mentioned in the previous section, the design of the power cells turned-out to have a direct

impact on the reliability. However, this was not the only aspect that required attention in order to achieve the expected reliability. The thickness of the thermal drain, but also the properties of the metal used for its fabrication also had a determinant role. As a consequence, several experiments were performed with varying process parameters to determine the optimum conditions. As an example, Figure 8 shows the reliability results obtained on a power transistor at an early stage of the optimization, clearly showing degraded lifetime. The best compromise regarding thermal drain thickness between minimum Rth and maximum lifetime was found to be 15µm.

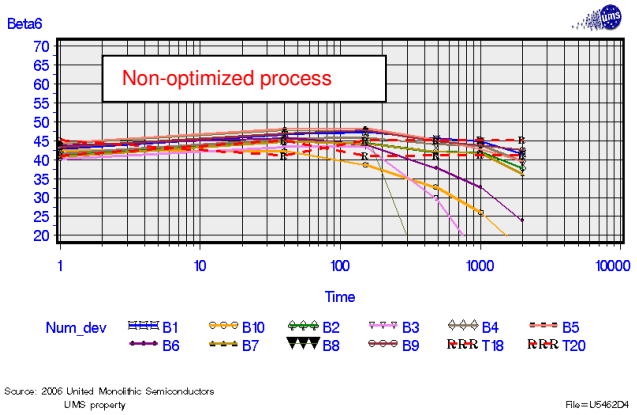

Figure 8: Current gain versus time (hours) of power cells under accelerated aging conditions (Tj = 223°C). Non-optimized process. (Red dashed lines are un-stressed reference devices).

Finally, through optimization of both power cell design and processing parameters, we were able to demonstrate the expected reliability level. Figure 9 shows the accelerated aging test result obtained for the optimum process. The test is still on going and no failure was observed after 6,000 hours.

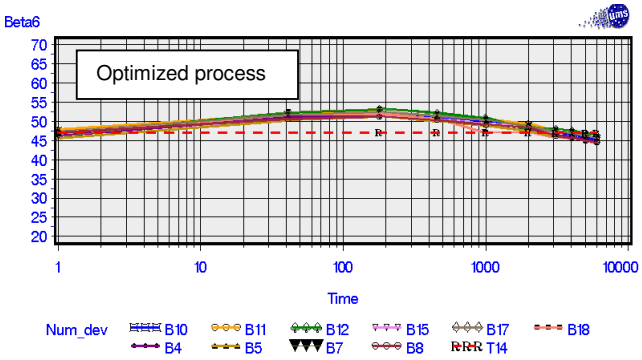

Figure 9: Current gain versus time (hours) of power cells under accelerated aging conditions (Tj = 223°C). Optimized process. (Red dashed lines are un-stressed reference devices).

CONCLUSIONS

UMS has developed a high power HBT technology for L- and S-Band applications. Special care was taken to optimize the performances and guarantee the same excellent reliability as our other HBT technologies. In particular, the power cell design played a decisive role in the optimization of both performance and reliability. With its, to our knowledge, unique features we believe that this technology is an excellent solution for specific applications to bridge the gap until alternative Wide-Bandgap-based technologies are really available and widely accepted.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
HPA: High Power Amplifier
PCM: Process Control Monitor
Rth: thermal resistance
BCce0: Emitter-collector breakdown voltage (3-terminal)
BCbc0: Base-Collector breakdown voltage (2-terminal)