0.10 µm Ion-Implanted GaAs MESFETs with Low Cost Production Process

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Keywords: Ion- implantation, Collimated Sputtering, GaAs MESFET, f_T, f_{max}

Abstract

We have successfully fabricated 0.1 µm gate GaAs MESFETs using a low cost process. The result was obtained from optical lithography, resist etching, and ion-implantation technologies based on Single Resist layer Dummy gate (SRD) process. The novel feature of the SRD process is forming a sub-quarter micron gate with conventional optical lithography. We have obtained a 0.18 µm gate using this process. Achieving a smaller gate length of 0.1um is very difficult with this process due to the pattern size shift of the sputtered SiO_2 opening. In this study, we use a collimated sputtering technique in the SRD process to reduce the pattern size shift. As a result, the pattern size shift of the SiO_2 opening decreases to 0.02 µm allowing a 0.1 µm gate length to be obtained by using conventional optical lithography. The high-speed performance of f_T =81 GHz and an f_{max} of 142 GHz are achieved with the refined SRD process.

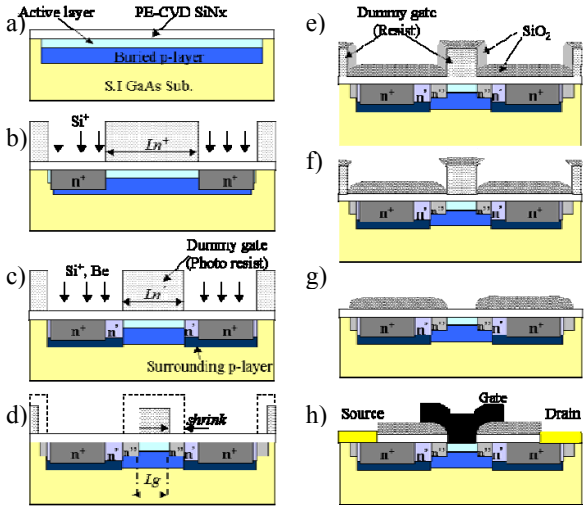


Fig. 1. Main fabrication sequence of SRD Process.

INTRODUCTION

High speed and low cost devices are eagerly required in the optical communication market. GaAs MESFETs have complied with this request by using different low cost processes. A self-aligned 0.1µm GaAs MESFET with Au/WSiN gate [1] and a 0.12 µm gate GaAs MESFET using blanket implantation and recessed gate structure [2] have been reported.

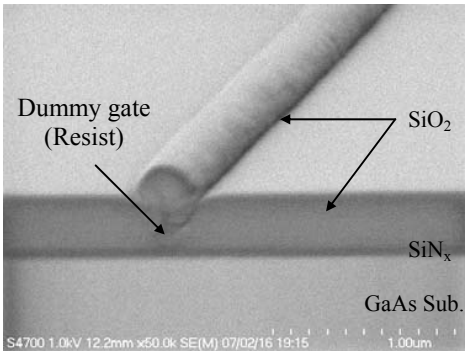
We have developed a Single Resist layer Dummy gate (SRD) process [3]. The novel feature of the SRD process is forming a sub-quarter micron gate with a simple and low cost process, *i.e.*, forming a sub-quarter micron gate with conventional optical lithography. In addition, MESFETs with the SRD process have a planar gate structure (not a recessed gate structure), so the process demonstrates excellent uniformity. We obtained a 0.18 µm gate using the SRD process. Achieving a smaller gate length of 0.1um is very difficult with this process due to the pattern size shift of the sputtered SiO_2 opening.

In this study, we use a collimated sputtering technique in the SRD process to reduce the pattern size shift. As a result, the amount of the pattern size shift of the SiO_2 opening decreases from 0.1 µm to 0.02 µm and we obtain 0.1 µm gate using conventional optical lithography. The high-speed performance of 81 GHz f_T and 142 GHz f_{max} is achieved with the refined SRD process.

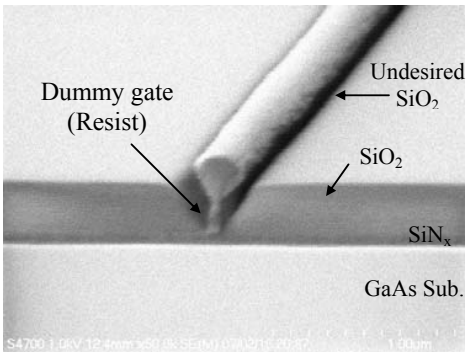
DEVICE FABRICATION PROCESS

The fabrication sequence of the SRD process is shown in Fig. 1. First, the active layers are selectively implanted by Si^+ and Be^+ with the acceleration energy of 10 and 70 keV, respectively (Fig.1-a). The carrier concentration of the buried p (BP)-layer is designed to be fully depleted in order to reduce the parasitic capacitance. A silicon nitride (SiN_x) film, which acts as an annealing cap, is deposited on the GaAs surface by plasma enhanced chemical vapor deposition (PECVD). After the SiN_x film deposition, an n^+

layer is selectively implanted by Si^+ at 100 keV (Fig.1-b). The sheet resistance of the n^+ layer is 200 ohm/square. The n' photoresist pattern with 0.6 μm thickness and 0.3 μm width is formed by an *i*-line stepper (Fig.1-c). For the lightly doped drain (LDD) structure formation, Si^+ is implanted at 60 keV in order to reduce the electric field at the drain side. Be^+ implantation for the surrounding p-layers is performed continuously at 90 keV in order to prevent leakage current from the source/drain regions. The n' pattern is shrunk (slimmed) by O_2 plasma etching to make the dummy gate (Fig.1-d). The width of the dummy gate is 0.08 μm. The n'' layers are implanted by Si^+ at 60 keV for the advanced LDD structure. A 3000 Å SiO_2 film is then sputtered on the pattern (Fig.1-e). The SiO_2 film adhering to the sidewall of the photoresist is removed by a BHF solution (Fig.1-f). After lifting-off the undesired photoresist and SiO_2, the activation annealing is performed by rapid thermal annealing to minimize the impurity diffusion (Fig.1-g). Finally, AuGe/Ni source/drain contacts and Ti/Pt/Au gate are formed by a conventional lift-off technique forming a self-aligned GaAs MESFET (Fig.1-h).



(a) Before BHF etching.



(b) After BHF etching (60 sec.).

Fig. 2. SEM cross-section of dummy gate using conventional SiO_2 sputtering.

PROCESS IMPROVEMENT BY COLLIMATED SPUTTERING

It is difficult to fabricate a 0.1 μm gate with the conventional SRD process due to the pattern size shift of the sputtered SiO_2 opening. The process is limited because the etching selectivity for BHF solution between the SiO_2 adhering to the sidewall of the photoresist and that on the other area (on a SiN_x or dummy gate) is not selective enough, therefore the SiO_2 opening becomes wider during this etching. The smallest gate length that can be achieved using this process is 0.18 μm which uses a 0.08 um dummy gate pattern.

The process requires 60 second SiO_2 etching with BHF solution to remove the SiO_2 adhering to the sidewall. The SEM cross-sections of the dummy gate after the SiO_2 deposition and the SiO_2 etching are shown in Fig. 2. As shown in Fig. 2 (b), the SiO_2 adhering to the sidewall is removed and photoresist is naked. It seems that the SiO_2 opening already becomes 0.18 μm at this step. The BHF solution etching time needs to be reduced in order for the pattern size shift of the sputtered SiO_2 opening to be smaller, therefore obtaining shorter gate lengths. Also, the SiO_2 adhering to the sidewall should be more porous to shorten the etching time and to achieve the narrow SiO_2 opening.

To accomplish this process enhancement, we chose a collimated sputtering technique. This technique helps make the SiO_2 adhering to the sidewall more porous. The collimated sputtering technique is applied in the process step shown in Fig. 1-e. The SEM cross-section of the dummy gate fabricated by the collimated sputtering after the BHF solution etching is shown in Fig. 3. In the conventional process, 60 seconds was required for the BHF solution etching, the improved process (using the collimated sputtering technique) requires only 12 seconds. Comparing the size of the undesired SiO_2 on the dummy gate in Fig. 2 (b) and Fig. 3, we can see that SiO_2 deposited by the

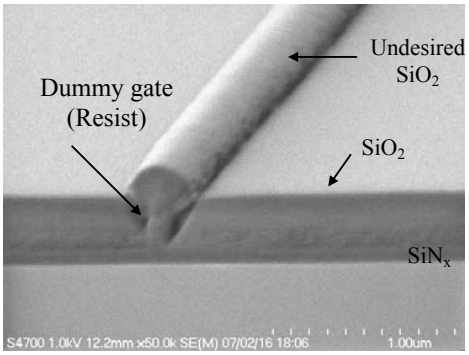


Fig. 3. SEM cross-section of dummy gate using collimated sputter after BHF etching (12 sec.).

collimated sputtering remains more than that deposited by the conventional sputtering after removal of the SiO_2 adhering to the sidewall.

Figure 4 shows the SEM photograph of the gate cross-section of the device fabricated with the collimated sputtering. To reduce the gate resistance, gold of the gate metal is deposited up to 0.8 µm thickness. As shown in Fig. 4, the gate length of 0.1 µm is obtained with the collimated sputtering and the conventional photolithography. The amount of the etching pattern size shift of the SiO_2 opening decreases from 0.1 µm to 0.02 µm.

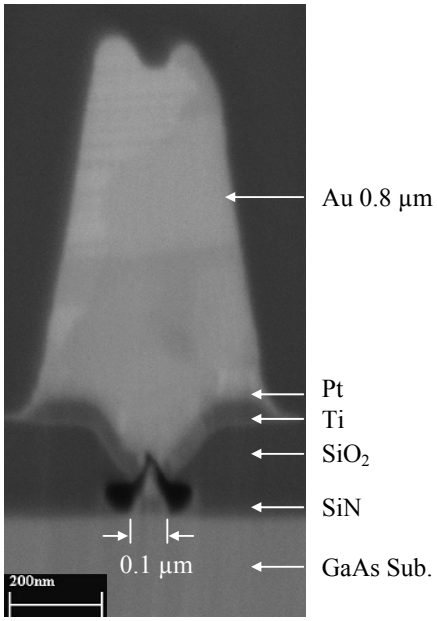


Fig. 4. SEM cross-section of FET gate region.

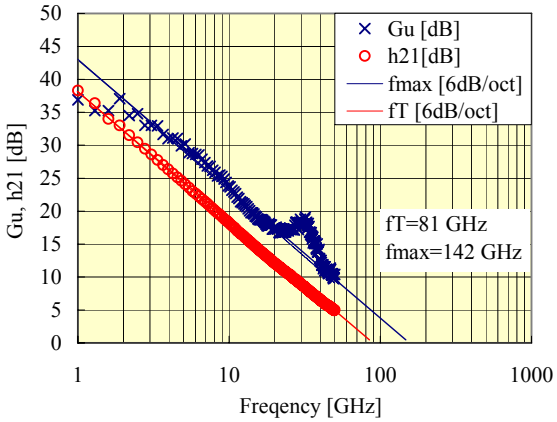


Fig. 5. Current gain and unilateral gain as a function of frequency.

Device Performance

Figure 5 shows the RF characteristics measured using an Agilent 8510C network analyzer for a 150um device (W_g = 2 x 75 µm) from 1 GHz to 50 GHz. An f_T of 81 GHz and an f_{max} of 142 GHz (without pad capacitance) are obtained under the bias condition of V_{ds} = 1.5 V and V_{gs} = 0.5 V. Typical I-V curves are shown in Fig. 6. Good pinch-off characteristics are observed. The high trans-conductance of 512 mS/mm and a breakdown voltage of 6.7 V are achieved.

Device Uniformity

Figure 7 shows the distribution of threshold voltage (V_{th}) of a 20-µm wide FETs over a 4-inch diameter wafer. The standard deviation of V_{th} is as small as 33 mV with an average value of -0.141 V. The excellent uniformity is due to the suppression of the short channel effect by the LDD structure and the fine control of the gate length by the SRD process.

Conclusions

We have improved the SRD process using the collimated sputtering technique to fabricate a 0.1 µm gate MESFET. As a result, the amount of the etching pattern size shift of the SiO_2 opening decreases from 0.1 µm to 0.02 µm and we obtained 0.1 µm gate length by using the conventional optical lithography. The high-speed performance of $f_{T=}$ 81 GHz and f_{max} =142 GHz was achieved with a 0.10 µm MESFET. This device has a high transconductance of 512 mS/mm and a breakdown voltage of 6.7 V. In addition, the standard deviation of V_{th} is as small as 33 mV with an average value of -0.141 V over a 4-inch diameter wafer. The results demonstrate that our ion-implanted MESFETs fabricated with the improved SRD process are suitable for low cost and high performance IC fabrication.

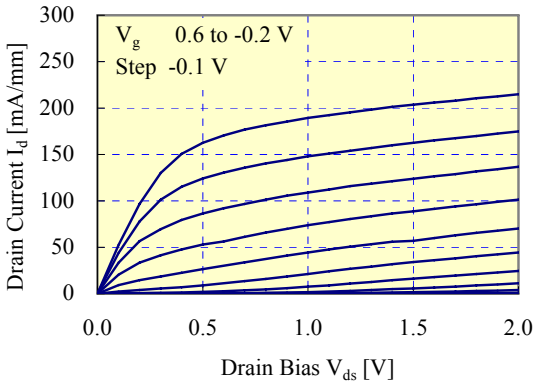


Fig. 6. I-V Characteristics of MESFET.

ACKNOWLEDGEMENTS

The authors would like to thank Seiji Yamanaka, TOKYO OHKA KOGYO CO., LTD. Additionally, support from the wafer processing division at Eudyna devices Inc. is appreciated.

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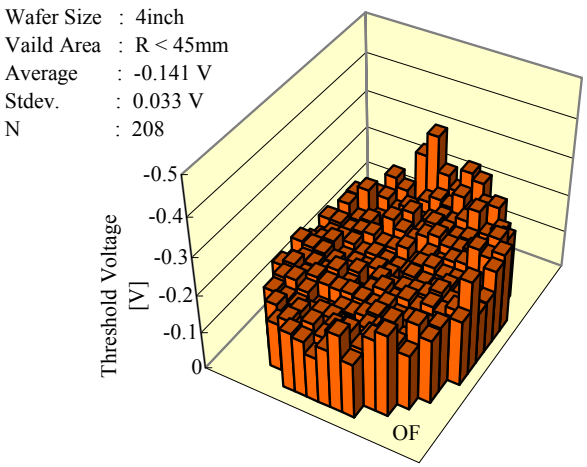

Fig. 7. Uniformity of the threshold voltage over 4-inch diameter wafer.