High-Voltage GaN-HEMTs for Power Electronics Applications and Current Collapse Phenomena under High Applied Voltage

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Abstract

Current collapse suppression in 380-V/1.9-A GaN power HEMTs designed for high-voltage power electronics application is reported. The current collapse is caused by the electron trapping by defects in the GaN layer and the interface between the passivation film and the AlGaN layer. Therefore the electric field at the gate edge strongly affects the collapse due to the acceleration of channel electrons. Three types of GaN-HEMTs with different design of the FP structure were fabricated to discuss the relation between the gate-edge electric field and the current collapse. It has been found that the optimized field plate structure minimizes the on-resistance increase caused by the current collapse phenomena. In addition, the on-resistance modulation was increased with the leakage current through the GaN layer. It implies that the accelerated electrons are trapped mainly in the GaN-layer defects. Crystal quality improvement of the GaN layer is also necessary to suppress the current collapse phenomena.

INTRODUCTION

Several hundred volts-class silicon power devices such as IGBTs and MOSFETs are widely used in power supplies, such as UPS's and motor drives. Characteristics of these devices have been improved to the level of the specific on-resistance $R_{on}A$ = 10 mΩ∗cm^2 (IGBT) to 20 mΩ∗cm^2 (MOSFET). Despite the recent improvement of silicon devices, further improvement of the specific on-resistance will become very difficult due to the silicon material property limitation.

As a future power device, high-voltage GaN HEMTs improve the trade-off characteristics between the on-resistance and the breakdown voltage dramatically thanks to both the high carrier mobility in 2DEG channel and the high critical electric field. Recently, high-voltage GaN-HEMTs have been demonstrated showing lower on-resistance than the Si-limit and large drain current operation [1]-[4].

Concerning transient operation of the GaN HEMTs, however, the conduction loss increasing with the current collapse phenomena is the major drawback, especially for high-voltage devices. The switching operation under high applied voltage is required in power electronics applications. The on-resistance increase by the current collapse phenomena degrades the power efficiency of the application circuit due to increase of the device conduction loss. In the previous works, however, the current collapse phenomena under high applied voltage have not been discussed.

The on-resistance increase caused by the current collapse phenomena strongly depends on the gate-edge electric field [5]. Therefore it can be expected that the current collapse is caused by the electron trapping by the high electric field acceleration. However, what has not been discussed is the main electron trapping position and the solution for suppressing the current collapse phenomena.

In this paper, the current collapse phenomena for high voltage AlGaN/GaN HEMTs will be discussed specially focused on power electronics applications. GaN power-HEMTs for 380-V/1.9-A operation are fabricated, and the current collapse phenomena under high applied voltage switching condition will be discussed.

DEVICE STRUCTURE

The GaN-HEMTs with FP electrode connected to the source electrode were fabricated as shown in Fig. 1. The FP structure was employed for suppression of the current

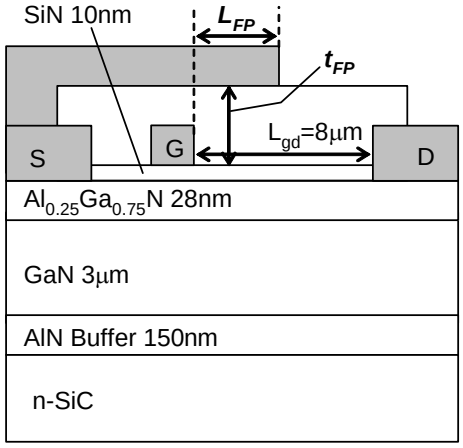

Fig. 1 Cross-sectional structure of the fabricated GaN-HEMT with MIS gate and FP structure.

collapse due to relaxation of the electric field concentration at the gate edge.

The expected mechanism of the current collapse phenomena is explained as follows. The 2DEG electrons are accelerated under high applied voltage. A part of the electrons is trapped at the defects in the GaN layer and the interface between the passivation film and the AlGaN layer. The trapped electrons are not released quickly even after turn-on state and deplete the 2DEG channel partially. As a result, the on-resistance is increased after applying the voltage. Therefore the electric field at the gate edge and the trapping density strongly affect the collapse phenomena.

Three types of the FP structure were fabricated to discuss the relation between the gate-edge electric field and the current collapse phenomena, as shown in Table 1. The electric field concentration at the gate edge is relaxed by the shielding effect of the FP structure. The shielding effect becomes strong with longer FP electrode and thinner insulator film under the FP electrode. Moreover, to discuss the electron trapping position, the devices were fabricated using two wafers, which have the same cross-sectional structure and different growth conditions.

The AlGaN/GaN heterostructure was grown on *n*-type 4H-SiC substrate by MOCVD. The heterostructure growth began with a 150 nm-thick AlN buffer layer, followed by 3 μm-thick undoped GaN layer as a channel layer. Finally, a 3 nm-thick undoped $Al_{0.25}Ga_{0.75}N$ spacer, a 20 nm-thick Si doped (5×10^{17} cm^{-3}) $Al_{0.25}Ga_{0.75}N$ carrier supply and a 5 nm-thick undoped $Al_{0.25}Ga_{0.75}N$ barrier layer were grown.

An MIS gate structure was employed to reduce the gate leakage current. The device processing consisted of conventional HEMT fabrication steps. First, as the gate insulator film, 10 nm-thick SiN was deposited using ECR-sputtering [6]. A Ti/Al layered metallization was evaporated and lifted off for source and drain ohmic contacts. The gate electrode was formed with Ni/Au. As the passivation film, SiN or SiN/ SiO_2 were deposited by CVD. Finally, the FP electrode was formed on the passivation film.

The gate-drain offset length was 8 μm and the gate length was 1 μm. The gate width was 3 mm. The active device area was 6.6×10^{-4} cm^2, which included source and drain contact regions.

STATIC CHARACTERISTICS

The fabricated HEMTs achieved maximum drain current of 1.9 A for a gate width of 3 mm, and specific on-resistance of 2 $m\Omega cm^2$, as shown in Fig. 2. The gate leakage current was dramatically reduced to less than 10nA/mm by the MIS gate structure, and the breakdown voltage was 380 V, as shown in Fig. 3.

Achieved $R_{on}A$-V_B trade-off characteristics of 2-$m\Omega cm^2$-380V correspond to about 10 times better than the Si-limit. The trade-off characteristics were independent of the FP structures because the FP structures do not influence 2DEG condition at low voltage, and the breakdown voltage is determined by the vertical electric field in the GaN layer between the drain electrode and the SiC substrate.

Table I. FP structure parameters for the fabricated GaN-HEMTs.

Device	Field Plate Length L_{FP}	Insulator Thickness t_{FP}
Type-A	4 μm	SiN 200nm
Type-B	4 μm	SiO_2 600nm /SiN 200nm
Type-C	2.5 μm	SiO_2 600nm /SiN 200nm

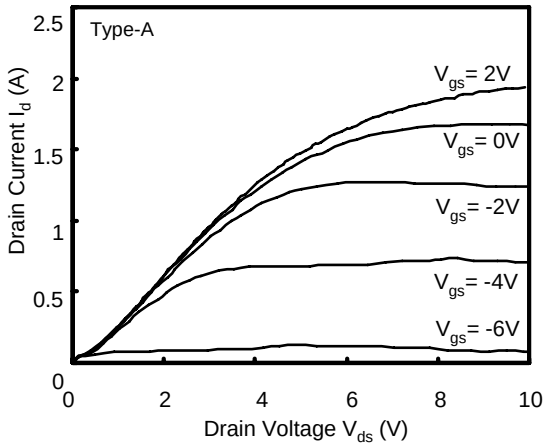

Fig. 2. On-state I-V curves of the fabricated GaN-HEMT.

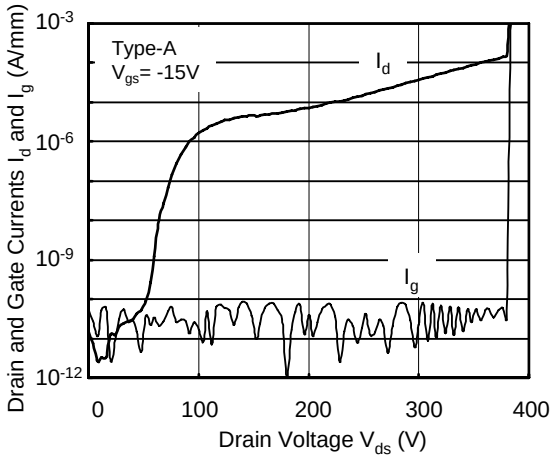

Fig. 3. Off-state I-V curves of the fabricated GaN-HEMT.

CURRENT COLLAPSE PHENOMENA SUPPRESSION

The on-resistance increase from applying high voltage measured from the on-state voltage at 10 kHz continues switching with resistive load. The on-state current was a constant of 0.4 A for various applied voltages by adjusting the load resistance.

The on-resistance was increased with the applied voltage and strongly depends on the FP structure as shown in Fig. 4. The on-resistance increase is decreased with the FP-structure shield effect, which becomes strong with longer FP electrode and thinner insulator film.

The electric field distributions under high applied voltage were calculated using device simulation [7]. The gate-edge electric-field peak is saturated under the applied voltage of over 100 V and the electric field concentration is relaxed by the FP-structure shield effect as shown in Fig. 5.

The tendency of the on-resistance increase shows good agreement with that of the gate-edge electric field. It is verified that the electron trapping is caused by the electric field related acceleration of the electrons at the gate electrode edge. The FP structure design is important to suppress the current collapse by the management of the electric field under high applied voltage.

To discuss the main trapping position at the current collapse phenomena, the relation between the static characteristics and the on-resistance increase was studied as follows.

It is expected that the accelerated electrons are trapped at the defects in the GaN layer and the interface between the AlGaN layer and the SiN film. The defect density in the GaN layer affects on the leakage current through the GaN layer. The interface trap at the SiN interface structure decreases the transconductance due to MIS-gate structure. Therefore the main trapping position can be expected using the relation between the static characteristics and the on-resistance increase.

The static characteristics for the devices fabricated using two wafers with different growth conditions were compared in this work, because the defect density in the GaN layer and the interface trap density at the AlGaN layer surface depend on the growth condition.

The transconductance was independent from the on-resistance increase under high applied voltage. Therefore, the interface trap density was independent from the growth condition and the accelerated electrons were trapped at the defects mainly in the GaN layer. Therefore the relation between the drain leakage current and the on-resistance increase is discussed as follows.

The measured drain-leakage currents under the applied voltage of 200 V for two wafers are shown in Fig. 6. The above experimental data are those for Wafer-A. For Wafer-B, the leakage current and its fluctuation are larger than those for Wafer-A and are suppressed by the increase of the FP-

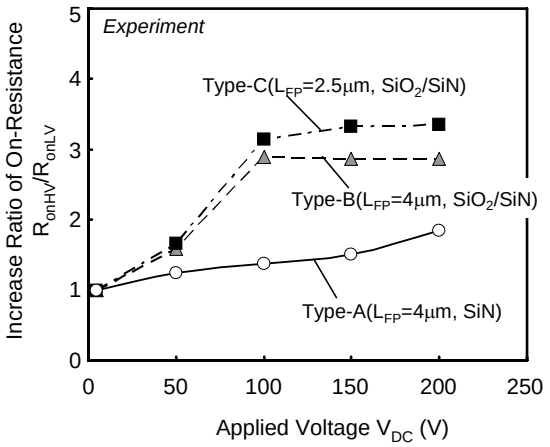

Fig. 4. Increase of the on-resistance with the applied voltage by the current collapse phenomena as a function of FP structure.

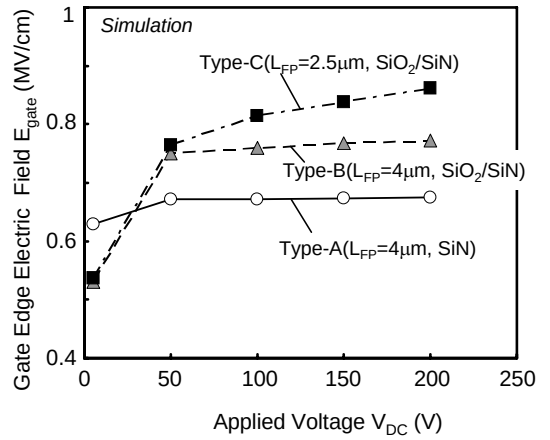

Fig. 5. Increase of the electric field at the gate electrode edge with the applied voltage as a function of FP structure.

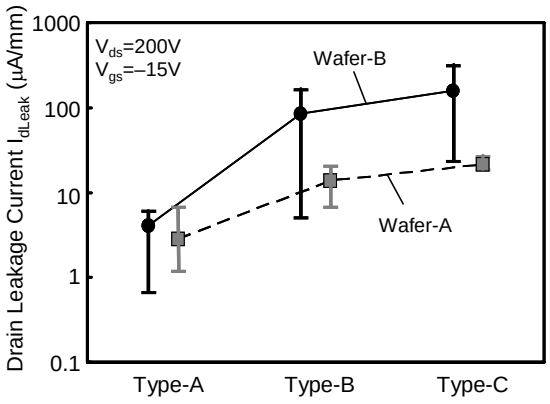

Fig. 6. Drain leakage currents for each wafer as a function of FP structure.

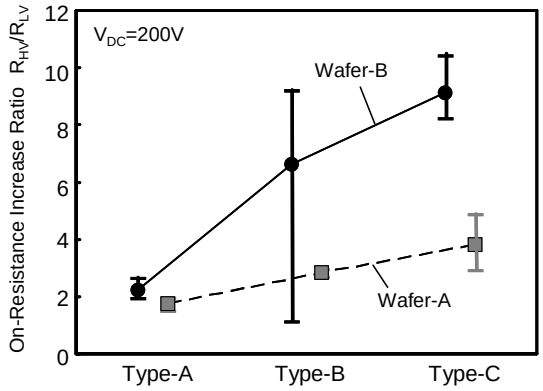

Fig. 7 On-resistance increase caused by the current collapse for each wafer as a function of FP structure.

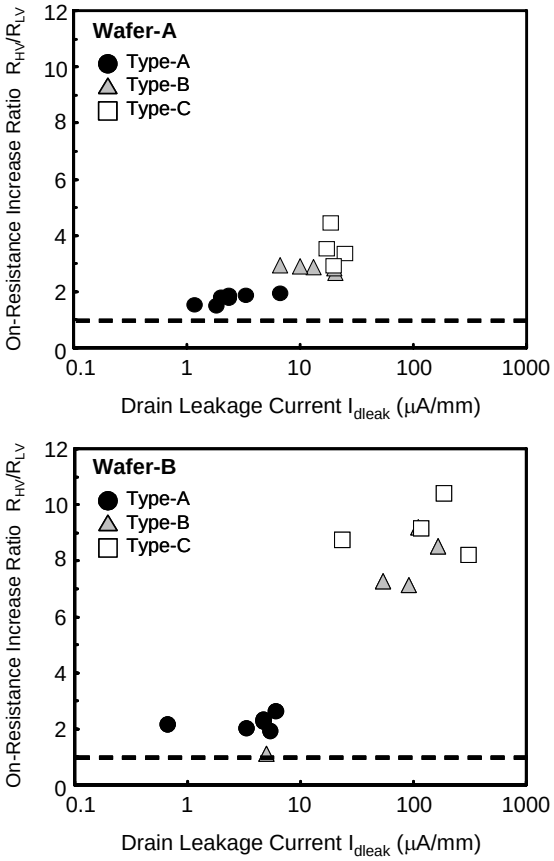

Fig. 8 Relation between the drain leakage current and the on-resistance increase caused by the current collapse.

structure shielding effect. The on-resistance increase for two wafers is compared as shown in Fig. 7. The on-resistance increase and its fluctuation for Wafer-B are also larger than those for Wafer-A.

From these results, for both of two wafers, the on-resistance increase was increased with the drain leakage current. Fig. 8 shows the relation between the on-resistance increase and the drain leakage current. Since the leakage current flows through the defects in the GaN layer, the large leakage current shows high defect density. Therefore these results imply that the accelerated electrons were trapped mainly in the GaN-layer defects.

In addition, the fluctuation of the on-resistance increase was suppressed by the optimal FP structure of type-A even for Wafer-B. The optimized FP structure minimizes not only the on-resistance increase but also its fluctuation. From these results, the current collapse phenomena can be suppressed by the optimized design of the FP structure and the improvement of the GaN-layer crystal quality due to reductions of the electron acceleration and the trapping center.

CONCLUSIONS

The on-resistance increase caused by the current collapse phenomena in high voltage GaN-HEMTs was measured. The FP structure is effective to suppress the current collapse, because the collapse phenomena are occurred by the electron trapping by the electric field acceleration at the gate edge. The device with the large leakage current through the GaN layer has large on-resistance increase caused by the current collapse. It is verified that the accelerated electron is trapped by defects mainly in GaN layer. The optimization of the FP design and the improvement of the GaN-layer crystal quality are necessary to suppress the current collapse phenomena.

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ACRONYMS

HEMT: High Electron Mobility Transistor
FP: Field Plate
2DEG: 2-Dimensional Electron Gas