Fabrication of a robust high-performance floating guard ring edge termination for power Silicon Carbide Vertical Junction Field Effect Transistors

Victor Veliadis, Megan McCoy, Ty McNutt, Harold Hearne, Li-Shu Chen, Gregory DeSalvo, Chris Clarke, Bruce Geil*, Dimos Katsis*, Skip Scozzie*

Northrop Grumman Advanced Technology Laboratory, MS 3B10, Linthicum, MD 21090
*U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, MD, 20783-1197, USA
Email: victor.veliadis@ngc.com, Phone: (410) 765-7037

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Abstract

Vertical Junction Field Effect Transistors were manufactured on 4H-SiC three-inch wafers for 1200 V power conditioning applications. To ensure high breakdown voltage yields, a robust high-performance guard ring edge termination was designed and fabricated. Manufacturing of the self-aligned guard ring structure requires relatively fewer processing steps and the occurrence of broken rings that lead to premature voltage breakdown is eliminated. The *p*+ guard rings are formed by multiple energy ion implantations, occurring simultaneously with the implantation of the *p*+ gates. The self-aligned property ensures excellent line-width control and precision in the distance of the first ring from the edge of the mesa. By optimizing the number of guard rings, their widths and spacings, and the proximity of the first guard ring to the main junction, breakdown voltages of 93% of the SiC material limit were obtained. This enables high voltage operation with minimum associated on-state resistance. Compared to the *Multiple Junction Termination Extension* technique, guard ring edge termination is more cost effective for manufacturing as it requires fewer processing and implantation steps.

INTRODUCTION

Silicon carbide (SiC) is ideally suited for power conditioning applications due to its high saturated drift velocity, its mechanical strength, its excellent thermal conductivity, and its wide band gap that results in high critical field strength. For power devices, the tenfold increase in critical field strength of SiC allows high voltage blocking layers to be fabricated significantly thinner than those of comparable Si devices. This reduces device on-state resistance and the associated conduction and switching losses, while maintaining the same high voltage blocking capability. Nevertheless, lack of proper edge termination can limit the potential performance of SiC power devices. Under reverse bias, planar junctions exhibit breakdown voltages well below the ideal SiC limit due to the effects of field crowding at the junction periphery. As a result, specialized edge termination structures must be implemented in order to obtain maximum breakdown voltage with relatively low associated on-state resistance.

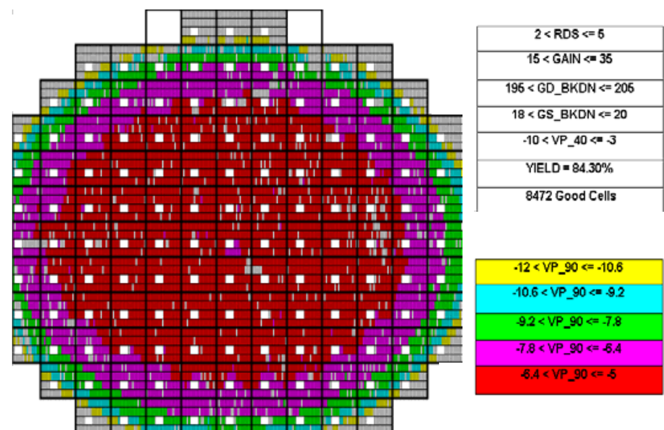


Figure 1: RF VJFET wafer map with 84.3% overall DC-yield. The screening parameter ranges appear on the right. Failed devices appear in gray. The "bulls-eye" structure corresponds to radial epitaxial doping non-uniformity, which is primarily responsible for rendering "edge" devices out of specification.

Previously, Northrop Grumman manufactured low-voltage RF Vertical Junction Field Effect Transistors (VJFETs) at high yields, (Figure 1), and with excellent wafer parameter uniformity [1]. To ensure high breakdown voltage yields in 1200 V power VJFETs, a robust high-performance, multiple floating guard-ring edge termination was designed and fabricated. The guard ring structure serves to reduce the amount of field crowding at the main junction by spreading the depletion layer past consecutively lower potential floating junctions (rings). These independent junctions act to increase the depletion layer spreading, thereby decreasing the high electric field at the main junction [2, 3]. The VJFET multiple floating guard ring structure was fabricated simultaneously with the *p*+ gate implantation. Compared to the *Multiple Junction Termination Extensions technique* [4], which has produced good results in SiC power devices, this floating guard-ring edge termination method does not require precise knowledge of the net implant activation percentages and can be implemented with fewer lithographic and processing steps, and fewer implantation steps. This results in a very attractive method for cost effective manufacturing.

High-voltage and normally-off SiC VJFETs were connected in the cascode circuit configuration to form a 1200 V, normally-off power switch. The cascode switch is an excellent candidate for high-temperature power conditioning applications such as the all-SiC 500 V half-bridge DC to AC inverter demonstrated by Northrop Grumman [5].

GUARD RING EDGE TERMINATION

p+ ion-implanted VJFETs were fabricated in 4H-SiC with a channel layer doped to low 10^{16} cm^{-3}, and a drift layer doped to mid 10^{15} cm^{-3}. To ensure >1200 V blocking, a 12μm drift layer thickness was chosen. The substrates and epitaxy were grown by commercial vendors. A cross section schematic of the VJFET structure is shown in Figure 2. In the on-state, majority carriers (electrons) flow vertically from source to drain. To control the current through the device the gates are subjected to a voltage, which adjusts the width of the depletion regions between the *p*-type gates in the *n*-type channel.

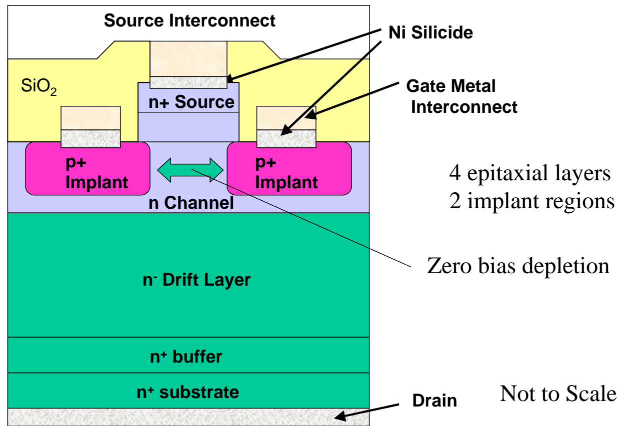


Figure 2: Cross-section schematic of a normally-on, ion-implanted SiC VJFET. The layer dimensions are not to scale.

Fabrication of the initial floating guard ring structures involved patterning resist rings, (Figure 3), depositing dielectric layers, performing a lift-off process, and reactive ion etching of dielectric, prior to *p+* ion implantation and thermal activation of the dopants. Resist type and thickness, exposure and development times, deposition and thickness of dielectric layers, and formation of a favorable resist undercut profile for lift-off, were all crucial in fabricating the guard ring design.

Using this process, Northrop Grumman successfully fabricated VJFETs that blocked 1600 V with a very low 2.1 mΩ-cm^2 associated on-state resistance [6]. However, the process complexities of this resist-dielectric guard ring method, combined with the challenging VJFET topography, resulted in frequent ring breaks, as shown in Figure 4. This lowered the breakdown voltage yields. In addition, variations in wafer flatness impacted ring widths and relative spacings, and limited the breakdown voltage.

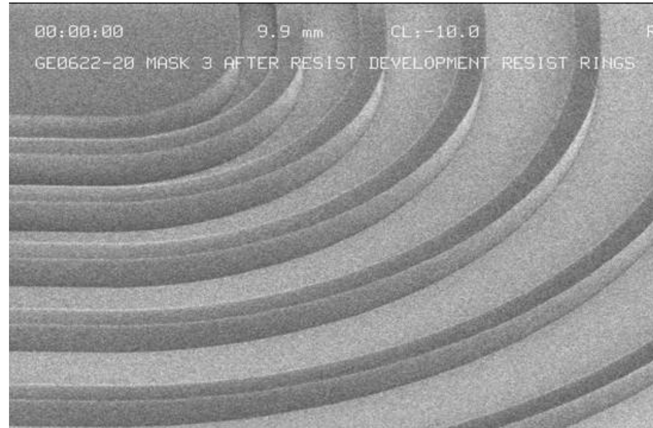


Figure 3: Scanning electron microscopy image of the resist ring structure used to form the floating guard ring edge termination.

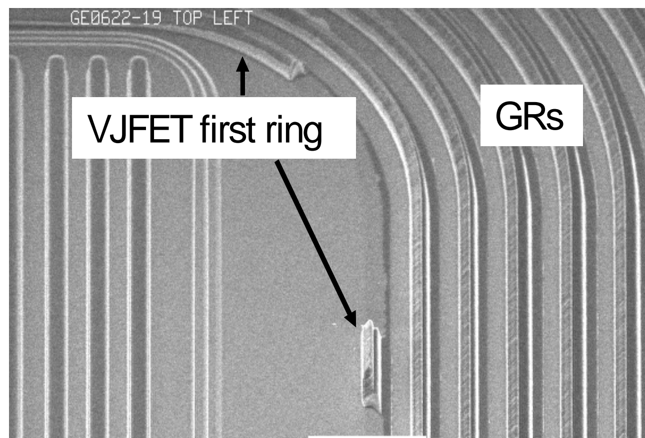
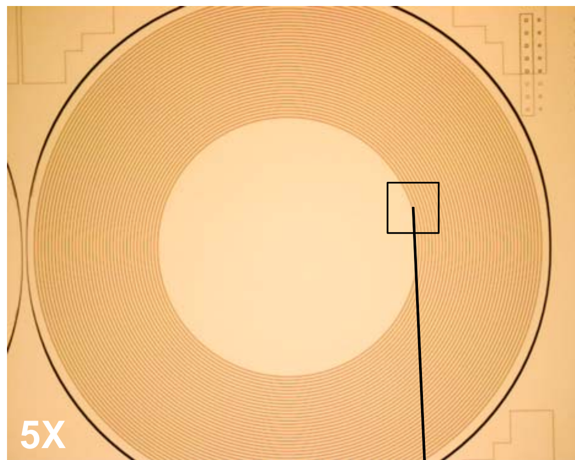


Figure 4: Scanning electron microscopy image of a guard ring edge termination structure in the periphery of the VJFET. The break in the first ring results in premature voltage breakdown.

To overcome the drawbacks of the resist-dielectric guard ring fabrication technique, a <u>self-aligned</u> guard-ring edge termination process was developed. This method minimizes the impact of variations in wafer flatness and in resist exposure and development times on guard ring line-width. The distance of the first guard ring from the edge of the VJFET mesa, a crucial parameter in maximizing breakdown voltage, is accurately maintained as the process is self aligned. The occurrence of broken rings, which is detrimental to breakdown performance, is virtually eliminated. Compared with the earlier resist-dielectric ring method, the self-aligned guard ring process ensures excellent line-width control and definition, reduces lithography by one to two mask levels, eliminates numerous processing steps, and produces a robust floating guard ring edge termination structure. A self-aligned guard ring test structure, consisting of thirty rings, is shown in the photographs of Figure 5. These self-aligned guard rings are representative of the process capability to controllably define narrow guard ring line-widths without any breaks.



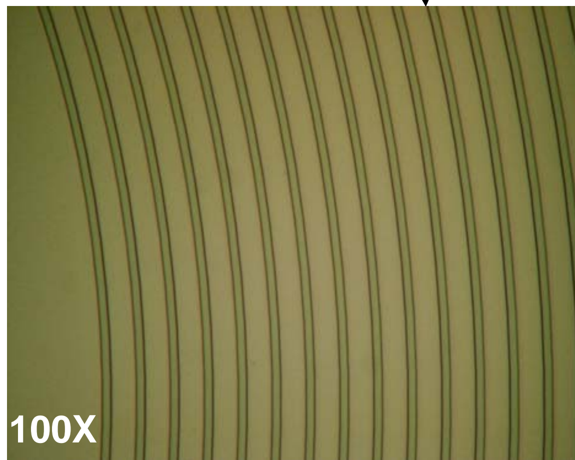


Figure 5: Optical microscopy images of a test structure consisting of thirty self-aligned guard rings. The process allows for excellent line-width control without breaks in the rings.

TESTING AND YIELDS

After silicide formation, VJFETs with self-aligned floating guard ring edge terminations were measured on-wafer using a Tektronix 371 curve tracer. The wafers were immersed in fluorinert and situated inside a Teflon dish during the high-voltage gate-to-drain measurements, as shown in the photograph of Figure 6.

To optimize the guard ring structure for high breakdown voltage, relatively small-sized test VJFETs with six different floating guard-ring designs were fabricated. The small size designs minimize the risk of premature breakdown due to the deleterious effects of material defects, and thus simplify evaluation of the high voltage performance capability of each design. Guard ring design parameter variations included the number of rings, their widths and spacings, and the proximity of the first guard ring to the main junction. Optimization of the first guard ring is crucial, as premature voltage breakdown due to electric field crowding in the first guard-ring renders the contribution of additional rings ineffective.

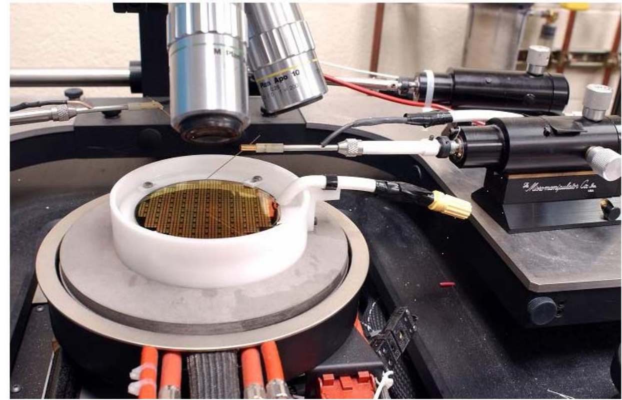


Figure 6: Wafer immersed in fluorinert for gate-to-drain high-voltage measurements after silicide formation.

The six different VJFET floating guard ring designs were included on all wafers. The drift layers had doping densities in the 3.5-4.2 X 10^{15} cm^{-3} range and were approximately 12 μm in thickness, which set the calculated SiC material breakdown limit at about 2175 V. The median breakdown voltage of each self-aligned guard ring design is shown in the histogram of Figure 7. In the absence of edge termination, the median VJFET breakdown voltage is 430 V and is denoted by the dashed line of Figure 7.

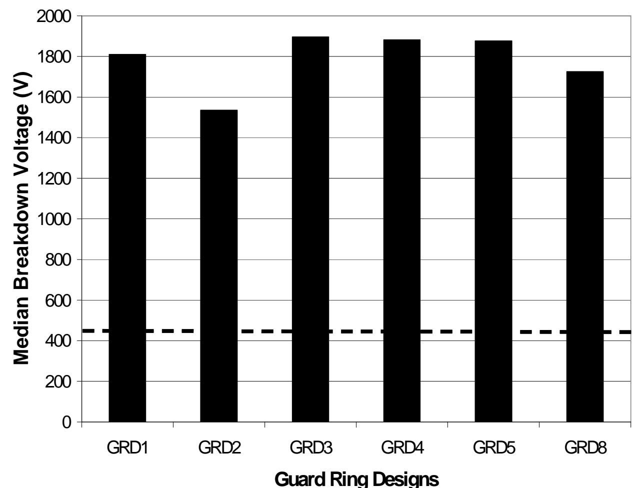


Figure 7: Median VJFET gate-to-drain breakdown voltages for the six floating guard ring edge termination designs. The high voltage measurements were performed after silicide formation on small area devices to minimize the contribution of material defects to voltage breakdown.

The self-aligned guard ring designs exploited trends for maximizing breakdown voltage that were heuristically established in previous fabrication runs. Breaks in guard rings, which had complicated determination of the optimum guard ring design in the past, did not occur in any of the wafers with self aligned guard rings. The optimal multiple

floating guard-ring structure "GRD3" withstood breakdown voltages of up to 2022 V, as shown in the measurement presented in Figure 8. This value corresponds to 93% of the calculated 4H-SiC material limit of the 11.79 µm drift layer, which was doped at 3.67 X 10^{15} cm^{-3}. It also represents a 470% improvement over breakdown voltages of VJFETs with no edge termination.

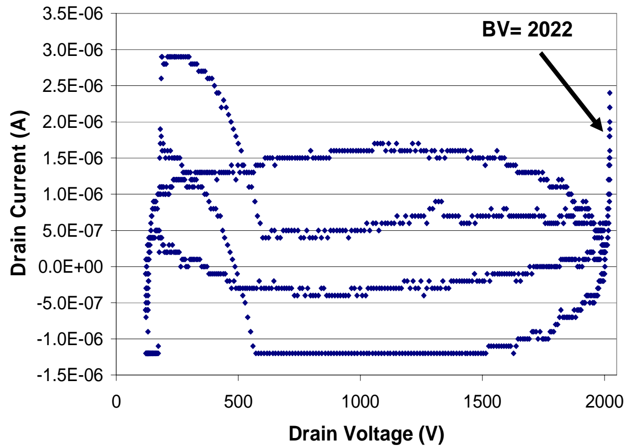


Figure 8: VJFET breakdown of 2022 V by use of the optimized self aligned floating guard ring structure. This value represents 93% of the calculated SiC material breakdown voltage limit.

The comparative breakdown-voltage advantage of the optimized self-aligned guard ring edge termination process is graphically shown by the frequency distributions of Figure 9.

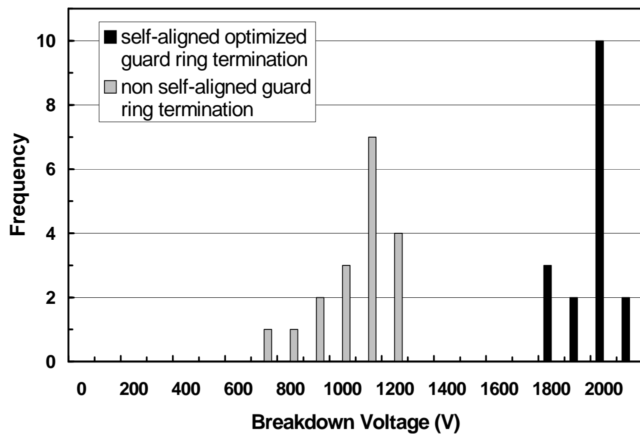


Figure 9: VJFET breakdown voltage distributions of the optimized self-aligned (black) and the non self-aligned (gray) floating guard ring edge termination processes. The self aligned process eliminates ring breaks and has excellent line-width control, which lead to superior breakdown performance.

The self-aligned guard ring process eliminates the occurrence of broken rings and allows for precise control of the distance of the first ring from the edge of the mesa. Furthermore, this new process enables evaluation of the breakdown voltage capability of different guard ring designs, as measured voltages are not skewed by breaks in rings and other fabrication imperfections. This leads to significant improvements in breakdown voltage performance and yields.

Although effective edge termination for SiC VJFETs was the primary focus of this effort, similarly high breakdown voltages were measured on *p-n* diodes that were also manufactured on these wafers. The optimized self-aligned guard ring termination is directly transferable to other SiC devices and is currently being implemented in Northrop Grumman's 1200 V power MOSFET wafers.

CONCLUSIONS

A robust, high-performance, self-aligned guard ring edge termination structure was designed and fabricated for SiC power devices operating in the 1200 V range. The process requires relatively fewer processing steps, eliminates the occurrence of broken guard rings, and allows for precise line-width control and definition. Breakdown voltages for the optimized guard ring structure reached 93% of 4H-SiC material limit. This enables high voltage operation with minimum associated on-state resistance. Implementation of the self-aligned guard ring edge termination process leads to significant improvements in breakdown voltage performance and yields.

ACKNOWLEDGEMENTS

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ACRONYMS

SiC: Silicon Carbide
Si: Silicon
VJFET: Vertical Junction Field Effect Transistor