III-V MOSFETs With Native Oxide Gate Dielectrics – Progress and Promise

P. Fay, X. Li, Y. Cao, J. Zhang, T. H. Kosel, and D. C. Hall

Dept. of Electrical Engineering, University of Notre Dame, 275 Fitzpatrick Hall,
Notre Dame, IN 46556. tel: (574) 631-5693, email: pfay@nd.edu

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Abstract

MOSFETs based on III-V channel materials have recently attracted considerable attention for possible use in high-speed and wireless applications. GaAs-based MOSFETs featuring native oxides of InAlP as the gate dielectric have recently been demonstrated for both enhancement- and depletion-mode operation, and with microwave performance comparable to conventional Schottky-gate HFETs. These devices leverage the extremely low gate leakage current and low interface state densities possible with the use of oxidized InAlP as the gate dielectric. Recent progress in the demonstration of GaAs-based MOSFETs using native oxides of InAlP as the gate dielectric is reviewed, the fabrication processing for these devices is described, and the material properties of these native oxides are discussed. The current status of the technology is presented, and prospects for future improvements in device performance are evaluated.

INTRODUCTION

Metal-oxide-semiconductor FETs (MOSFETs) with high-mobility III-V channels are of significant interest for use in high-speed circuits. Conventional III-V FETs rely on the use of a Schottky contact for the gate, resulting in significant gate leakage and a limited positive gate voltage due to gate turn-on. With the use of an insulating gate as in a MOSFET, the gate leakage–and more importantly the gate diode turn-on–can be eliminated. This promises to produce devices with significant performance and circuit advantages over conventional HEMT and HFET structures, including enhancement-mode devices operable with appreciable positive voltages on the gate. Applications including power amplifiers, switches, and high-speed logic could benefit from such a device.

As a consequence of the circuit-level appeal of such a device, many efforts spanning several decades have been devoted to attempts to realize high-quality III-V MOSFETs. While MOSFETs on Si have been a well-established technology for many years, the more complex nature of oxidation on compound semiconductor materials as well as fundamental differences in the material properties have resulted in much slower progress for III-V based devices. Recently, however, III-V MOSFETs with promising performance have been demonstrated using a range of gate dielectric materials and fabrication processes. MOSFETs with MBE-grown $Ga_2O_3/(Gd_xGa_{1-x})_2O_3$ [1-3] or atomic layer deposition (ALD)-grown Al_2O_3 [4] for the gate dielectrics have been reported. As an alternative to deposited gate dielectrics, the use of native-oxide films in GaAs-based MOSFETs has also been explored. Although the use of native oxides of GaAs and AlGaAs as gate dielectrics can lead to high interface state densities and thus poor MOSFET performance, the use of the native oxide of InAlP as the gate dielectric has recently been shown to offer significant advantages over other native oxides [5]. Gate leakage current densities comparable to the best reported results with deposited dielectric films have been achieved, modest measured interface state densities have been obtained [6], and MOSFETs with RF performance approaching the intrinsic limits have been demonstrated [7-8]. The use of native-oxide films as the gate dielectric also offers advantages in fabrication process integration, and may provide a low-cost approach to implementing III-V based MOSFETs.

In this paper, the performance of MOSFETs fabricated using native oxides of InAlP as the gate dielectric is reviewed. Devices operating in both depletion and enhancement modes have been demonstrated, and the obtained DC and RF results are consistent with theoretical expectations for GaAs-channel devices at the gate geometries evaluated. The prospects for further improvement of the technology are also examined.

DEVICE STRUCTURE AND FABRICATION

Several different designs for MOSFETs with InAlP native oxide as the gate dielectric and GaAs as the channel material have been demonstrated. Figure 1 shows cross-sectional diagrams of two typical heterostructures; Fig. 1(a) shows the heterostructure for a depletion-mode device and

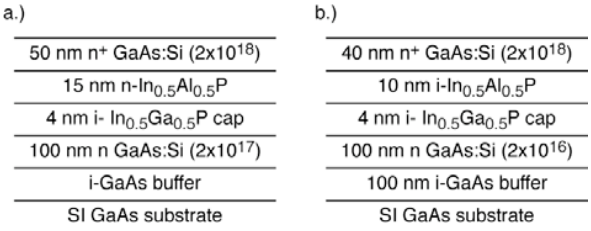

Figure 1. Cross-sectional diagram of heterostructures for (a) depletion-mode and (b) enhancement-mode GaAs-channel MOSFETs.

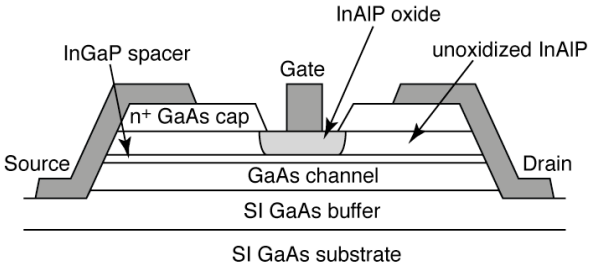

Figure 2. Cross-section of InAlP-oxide based MOSFET.

1(b) illustrates an enhancement-mode MOSFET. These doped-channel epitaxial structures were grown by MOCVD, and each structure was grown in a single uninterrupted growth run. As can be seen in Fig. 1, the primary differences between these E- and D-mode MOSFET structures are the doping level in the channel and the thickness of the gate dielectric. The channel mobility in the enhancement-mode and depletion-mode structures were measured to be 3200 cm^2/Vs and 3310 cm^2/Vs, respectively.

Fabrication of MOSFETs based on these heterostructures is similar to fabrication of conventional Schottky-gate HFETs or HEMTs, with the key distinction that a thermal oxidation step is introduced in the MOSFET fabrication. A number of variations on the fabrication processing have been explored; Figure 2 shows a schematic cross-section after a typical process flow. For the cross-section shown in Fig. 2, the devices are mesa isolated using a sequence of selective wet etches; HCl-based etchants are used for the phosphides, while citric acid/hydrogen peroxide solutions are used to etch the arsenides. To form the gate dielectric, the n^+ GaAs cap layer is selectively removed in the gate region by wet chemical etching in a citric acid/hydrogen peroxide solution. This etch is extremely selective, resulting in wide process margin for removing the GaAs cap without appreciably thinning the InAlP. The InAlP is then oxidized only in regions where the cap has been removed, with the GaAs cap acting as a mask against oxidation. This "local oxidation" process is performed in a tube furnace at 440 °C in a water vapor/N_2 ambient. The water vapor is supplied by bubbling ultra-high purity N_2 through a water bath held at 95 °C. The InGaP spacer layer acts as an oxidation stop layer, preventing any oxidizing species from reaching the GaAs channel. Ohmic contacts for the MOSFET source and drain are formed by thermally evaporating and lifting off AuGe/Ni/Au films and annealing the contacts by RTA, and gates are formed by conventional lithography and liftoff of either Cr/Au (depletion-mode) or Ti/Au (enhancement-mode). The native oxide of InAlP is quite robust and is not affected by the contact anneal; preliminary studies indicate that these heterostructures can withstand anneals at 880 °C (e.g. typical of implant activations) without discernible degradation in their electrical characteristics.

DEVICE PERFORMANCE

Devices fabricated on the heterostructures shown in Fig. 1 were characterized at both DC and RF. Figure 3 shows a typical common-source characteristic for an enhancement-mode MOSFET with a 2 µm gate length and 100 µm gate width fabricated on the heterostructure in Fig. 1(b), while Figure 4 shows the drain current and transconductance of this device as a function of gate voltage. The device exhibits a threshold voltage of 0.15 V. The peak extrinsic transconductance of the device is approximately 24 mS/mm. This low extrinsic transconductance arises due to a substantial parasitic source resistance. This parasitic resistance results from the partially-depleted channel between the edge of the gate and the source-side edge of the local oxidation window due to the relaxed alignment tolerances used. In this device, approximately 1.5 µm of the gate-source space was oxidized, while for an optimized process this distance should be minimized. Accounting for this resistance, the device's intrinsic transconductance is 63.8 mS/mm, consistent with expectations for a doped GaAs channel with this doping level [9].

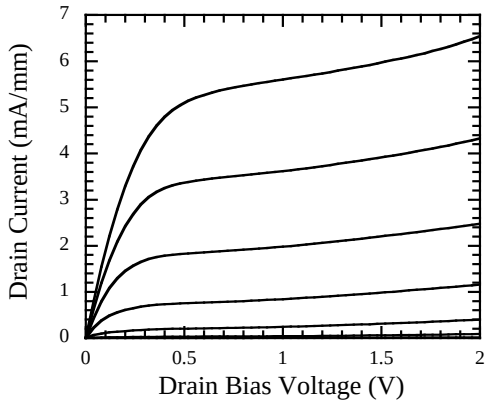

Figure 3. Common-source characteristics of enhancement-mode MOSFET with 2 µm gate. Gate voltage stepped from -0.2 V to 0.5 V in 0.1 V steps.

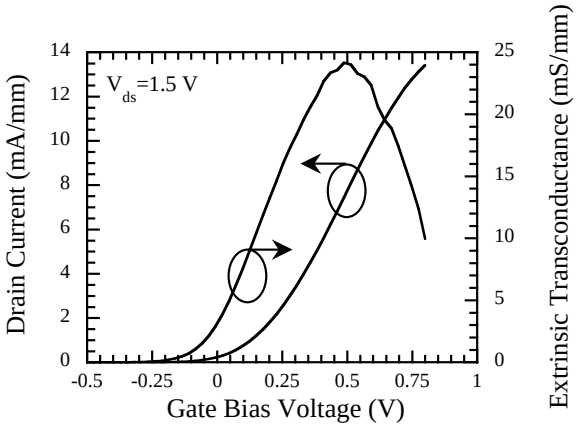

Figure 4. Drain current and extrinsic transconductance as a function of gate voltage for 2 µm gate length enhancement-mode MOSFET.

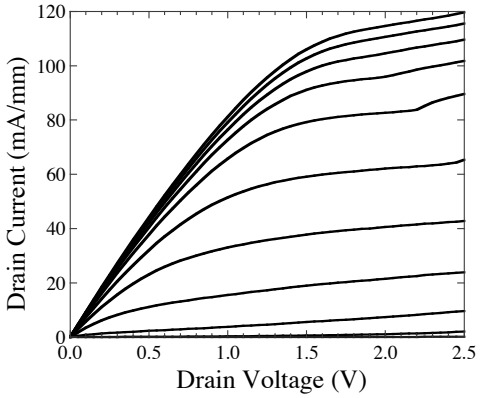

Figure 5. Common-source characteristics of 1 μm gate length, 100 μm gate width depletion-mode MOSFET.

Figure 5 shows the measured common-source characteristics for a typical 1 μm gate length depletion-mode device fabricated with the heterostructure illustrated in Fig. 1(a), and Figure 6 shows the corresponding drain current and transconductance characteristics. The gate width for this device is also 100 μm. The threshold voltage of this device is -2.4 V, with a peak extrinsic transconductance of 74 mS/mm. Due to the higher doping level in this structure, the source resistance is significantly reduced compared to the E-mode device shown in Figs. 3 and 4; however, since these devices still include a significant region of higher-sheet resistance material in the channel between the gate edge and the source-side edge of the local oxidation window, a parasitic source resistance is still present. This reduces the extrinsic transconductance; the intrinsic transconductance of this device is 129 mS/mm.

It is worth noting that the transconductance of these devices, while lower than that of typical HEMTs of comparable gate length and gate-to-channel distance, is consistent with the expected trend given by the transconductance relationship $\mu C_{ox}(W/L)$ where μ is the effective channel mobility, C_{ox} is the gate oxide capacitance per unit area, W is the gate width, and L is the gate length. The transconductance parameter, $k_n=\mu C_{ox}$, is not expected to exactly equal the channel mobility–gate capacitance product for these devices due to simplified underlying assumptions in its derivation (long gate length, no velocity saturation), but k_n does offer a convenient metric for comparing different device technologies. The k_n value inferred from the peak intrinsic transconductance for these native-oxide enhancement-mode devices is 0.899 mS/V, in reasonable agreement with 1.16 mS/V from direct multiplication of the measured channel mobility and gate capacitance. The k_n for these native oxide devices are also comparable to results reported for devices fabricated using MBE-grown oxides [3], after correcting for the lower dielectric constant of InAlP oxides compared to the gadolinium gallium oxide and the lower channel mobility due to the lattice matched and doped GaAs channel used here compared to the pseudomorphic channel used in [3]. This indicates that these devices are governed by the conventional expressions for HFETs and MOSFETs, and that interface states do not appear to play a significant role in the performance of the InAlP native-oxide based devices.

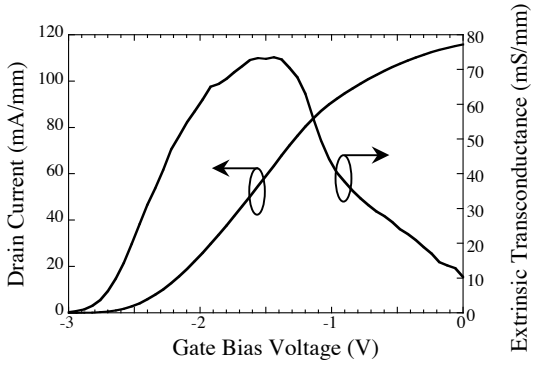

Figure 6. Drain current and transconductance vs. gate voltage for 1 μm gate length depletion-mode MOSFET.

The gate leakage currents of these devices were also characterized. Figure 7 shows the measured gate leakage for the depletion-mode MOSFET shown in Figs. 5 and 6, as well as the measured leakage current for a much larger-area capacitor test structure. As is evident in Fig. 7, the leakage current of the MOSFET is considerably higher than that of the much-larger MOS capacitor structure, but the gate current density at 1 V bias (20 μA/mm) is still approximately 5 orders of magnitude smaller than that of a typical HEMT Schottky gate of the same gate length. The larger gate current in the MOSFETs compared to the MOS capacitor test structures arises from the contact of the gate to the channel at the mesa edges, a feature that is not present in the capacitor test structures.

The microwave performance of the devices has also been characterized. Figure 8 shows a typical measured current gain and maximum available gain characteristic for a 1 μm gate length, 100 μm gate width depletion-mode device. An f_t of 17 GHz and f_{max} of 74.8 GHz is obtained, indicating that

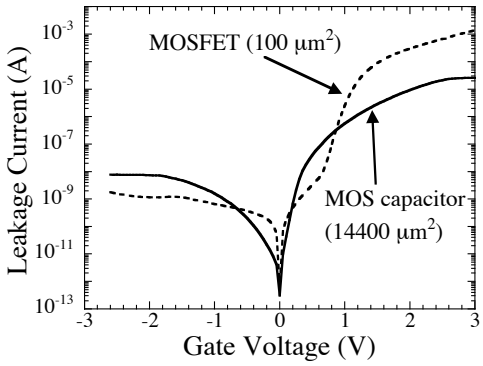

Figure 7. Leakage current of MOSFET gate and MOS capacitor test structure. MOSFET exhibits higher leakage due to gate contact with mesa edge, while MOS capacitor reflects intrinsic oxide leakage.

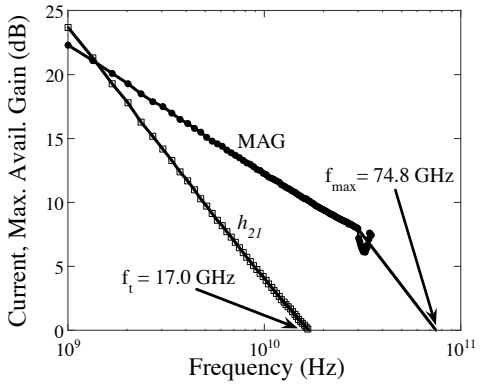

Figure 8. Microwave performance of typical 1 μm gate length depletion mode device.

the device performance is consistent with theoretical expectations for a lattice-matched GaAs channel of this gate length. Measurements of enhancement-mode devices resulted in somewhat lower performance, consistent with the large source access resistances.

PROSPECTS FOR DEVICE IMPROVEMENTS

The devices demonstrated to date suggest that native oxides of InAlP are a potentially interesting gate dielectric material for GaAs-based MOSFETs due to the resulting combination of very simple fabrication processing and promising device performance. Furthermore, the device heterostructures and fabrication processes have not yet been optimized. There are several opportunities for improving device performance that can be easily envisioned to make these devices competitive with mainstream HEMTs while maintaining the advantages of a MOSFET structure. The first of these is the implementation of a self-aligned process to reduce the length of the oxidized region between gate and source. A second opportunity for device improvement is the reduction in the oxide thickness to improve the transconductance (by increasing C_{ox}) as well as to permit MOSFETs with shorter gate lengths to be fabricated without suffering from short-channel effects. Since the dielectric constant of the native oxide of InAlP is 6.57 [10], the thickness of the oxide should be approximately half that of the Schottky barrier layer in an equivalently-scaled GaAs HEMT. InAlP native oxide films as thin as 7.5 nm have been fabricated and found to produce low leakage current densities, indicating that this scaling is feasible. The use of undoped, pseudomorphic InGaAs channels for higher mobility is another area for future improvement of these devices.

CONCLUSIONS

The performance of GaAs-channel MOSFETs using the native oxide of InAlP as the gate dielectric has been reviewed. Despite the comparatively early stage of this device development, the MOSFETs demonstrated to date suggest that these devices may provide advantages for some systems, and a clear path to improved device performance can be seen. The InAlP oxides may enable simple, low-cost, fabrication approaches to produce GaAs-based MOSFETs for commercial systems.

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ACRONYMS

HFET: Heterostructure Field-Effect Transistor
HEMT: High-Electron Mobility Transistor
MBE: Molecular Beam Epitaxy
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
MOCVD: Metal-Organic Chemical Vapor Deposition
RTA: Rapid Thermal Annealing