Post-Si CMOS: III-V n-MOSFETs with High-k Gate Dielectrics

Yanning Sun,[1] S. J. Koester,[1] E. W. Kiewra,[1] J. P. de Souza[1], N. Ruiz,[1] J. J. Bucchignano,[1] A. Callegari,[1] K. E. Fogel,[1] D. K. Sadana,[1] J. Fompeyrine,[2] D. J. Webb,[2] J.- P. Locquet,[2] M. Sousa,[2] R. Germann,[2]

[1]IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598, USA, yansun@us.ibm.com, (914) 945-3083
[2]IBM Zürich Research Laboratory, CH-8803 Rüschlikon, Switzerland

Keywords: III-V, MOSFET, BURIED-CHANNEL, ENHANCEMENT-MODE, HIGH-K, DIELECTRIC

Abstract

As the end of Si CMOS scaling is approaching, III-V compound semiconductors have received renewed attention as the channel materials for future generation CMOS technology. We have reviewed the benefits, the opportunities, and the challenges of III-Vs for digital applications. We have also demonstrated functional enhancement-mode GaAs- , and InGaAs- channel MOSFETs, with high-① gate dielectrics. The results show promise for realizing III-V MOSFETs for future VLSI logic applications.

INTRODUCTION

For the last few decades, Si CMOS technology has been driven by device scaling to increase performance, as well as reduce cost and maintain low power consumption. However, as devices are scaled below the 100 nm region, performance gain has become increasingly difficult to obtain by traditional scaling. A paradigm shift has been occurring in the industry, where materials innovation, rather than scaling, is becoming the primary enabler for performance enhancement in CMOS technology as show in Fig. 1. For gate materials, traditional SiO_2 is being replaced by high-① dielectrics to reduce the gate leakage current. Even more drastic materials innovation is the incorporation of high mobility channel materials. High mobility materials can greatly improve the power /performance tradeoff which is a tremendous advantage for VLSI digital applications. Currently in industry, mobility enhancement is achieved by applying strain to conventional Si MOSFETs, either through process-induced strain [3] or substrate engineering [4]. However, the mobility benefits that can be achieved by straining Si are limited and reduced by scaling, and there is great interest in studying non-Si channel materials to achieve even higher mobilities.

III-V BENEFITS AND OPPORTUNITIES

Compound III-V materials are attractive for achieving enhanced NFET mobility, due to their high bulk electron mobility. As shown in Fig. 2. for a given electric field, III-V materials can have higher velocity compared to Si. On the other hand, the equal velocity can be achieved at a lower applied voltage for III-V materials. These advantages can

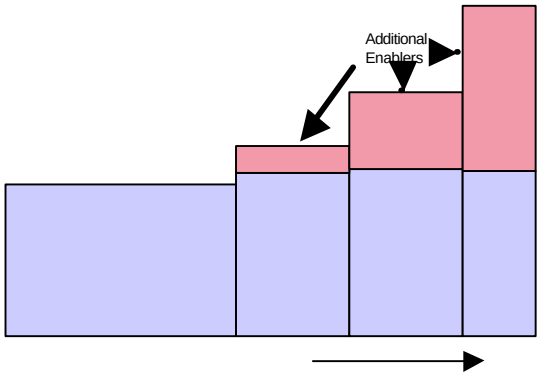


Fig. 1. CMOS performance scaling landscape [1]

bring tremendous benefits in terms of circuit and system performance due to the improved power/performance tradeoff. Having higher electron mobility, III-V channel nMOSFETs can achieve performance enhancement, as well as reduced dynamic power consumption for a fixed performance level.

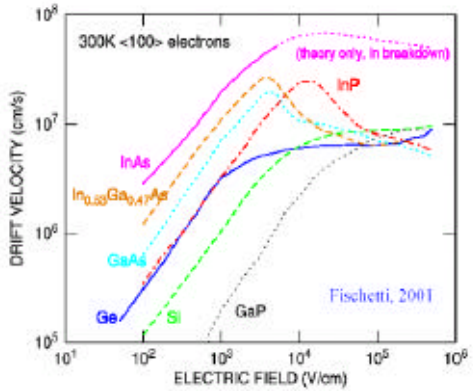


Fig. 2. Electron drift velocity vs. electric field for various semiconductors [2]

III-V compound semiconductors also have the advantage of a lattice matched hetero-structure material system with a wide selection of band gaps and materials. Compared to Si-based hetero-structures such as Si/SiGe, the III-V hetero-structures allow much greater flexibility in band structure engineering and thereby device design for both high-performance and low power applications.

Presently, compound III-V materials are mainly used for communications and opto-electronic applications. They have not received serious consideration for digital applications in the past years, due to the lack of high quality native oxides, as well as the success of Si CMOS. However, with the end of Si device scaling approaching, and non-traditional materials being increasingly incorporated into mainstream Si technology, III-Vs are receiving renewed attention as channel materials for VLSI logic applications.

III-V CHALLENGES

The main challenges in implementing III-V channels for manufacturing CMOS technology are as follows: first, III-V materials do not have an effective gate stack solution. Unlike Si, the native oxides of III-Vs have very poor electrical properties, which make both the thermal and the deposited oxides problematic due to the difficulty in completely removing the native oxide prior to the gate dielectric deposition. Despite some progress in recent years [5]-[10], the problem of forming a high-quality gate insulator remains a significant barrier to implementing III-V for CMOS applications.

Second, III-V substrates are expensive, brittle and difficult to make in large sizes. Furthermore, from an economics point of view, the success of any future CMOS technology with non-Si channels will depend on its compatibility with the existing Si manufacturing infrastructure. Therefore, methods need to be developed to integrate III-V channels on Si substrates, which can be possibly achieved through either wafer bonding or epitaxial growth. However, both methods are quite challenging due to large thermal and lattice mismatch, and the formation of anti-phase domains.

Third, III-V materials do not have a superior hole mobility compared to Si. However, III-Vs still have the net mobility advantage over Si for CMOS application due to their much higher electron mobility, and lightly lower or comparable hole mobility. Nevertheless, a better integration scheme is to utilize III-V for the NFET and Ge for the PFET due to the high hole mobility of Ge. In addition, some III-Vs like GaAs are almost lattice matched to Ge. Other issues such as the low conduction band density of states and the low n-type doping are also potential problems for III-Vs.

Among all these challenges, perhaps an effective gate stack solution is the most imperative. In this paper, we address this issue by investigating surface passivation techniques, as well as the device design. In addition, the integration scheme of III-V MOSFETs is also reported.

III-V DEVICE STRUCTURES

There are primarily two III-V MOSFET structures under study for digital application, surface-channel MOSFETs and buried-channel MOSFETs. Buried-channel MOSFET typically has a quantum well epi-structure where there is a wide band-gap material layer between gate and channel. While surface-channel devices are more desirable to achieve higher inversion capacitance, they require the formation of a very-high-quality semiconductor-dielectric interface in order to preserve low interface-state density near the surface-layer conduction-band edge. For this reason, a buried-channel MOSFET design may be preferable, to relax the requirements for low interface-state density near the surface-semiconductor conduction-band edge, as well as improve the carrier mobility. However, the capacitance penalty due to a buried channel will offset some of the advantages provided by the high mobility, and it is important to examine the performance trade offs between the surface and buried channels designs. Recent work on both device structures at IBM by Koester et al. [13] [14], and Sun et al. [15] demonstrates (i) Carrier inversion in n- and p-type GaAs MOS capacitors with HfO_2 gate dielectrics and a-Si/SiO_2 interlayers, (ii) Enhancement-mode self-aligned GaAs MOSFETs with HfO_2 gate dielectrics, and (iii) $In_{0.7}Ga_{0.3}As$ buried-channel MOSFETs using HfO_2 dielectrics.

GALLIUM ARSENIDE SURFACE-CHANNEL MOSFETS

GaAs is attractive as a III-V channel material, due to its high electron mobility (~ 6x compared to Si), its approximate lattice matching with Ge, and its relative maturity compared to other compound semiconductors. One of the major challenges of implementing GaAs surface-channel MOSFETs is to form a high-quality gate dielectric with low interface state density [5]-[10] However, other problems also need to be overcome, including poor thermal stability, low implant activation, and lack of a self-aligned contacting scheme.

Passivation of the GaAs surface using α-Si has been investigated to improve the thermal stability and D_{it} of the HfO_2/GaAs interface [13]. The GaAs wafer was loaded into an MBE system after wet-cleaning. Atomic H was then applied to remove the native oxide, followed by *in situ* deposition of α-Si. The sample was then removed from MBE, and 10 nm HfO_2 was deposited by ALD at 300 ^oC. The corresponding MOS capacitors showed C-V characteristics with D_{it} values of 7 x 10^{11} cm^{-2}/eV, roughly an order of magnitude lower than the capacitors with HfO_2 directly on GaAs. Capacitors with α-Si/SiO_2 interlayers on p-type GaAs were also investigated. These structures utilized MBE-deposited HfO_2 that was deposited *it situ* after α-Si deposition. Inversion was confirmed on both *n*- and *p*-type GaAs MOS capacitors by low-frequency (100 Hz) C-V measurements using illumination of a dot capacitor fabricated with an opaque Al dot electrode, as shown in Fig.3.

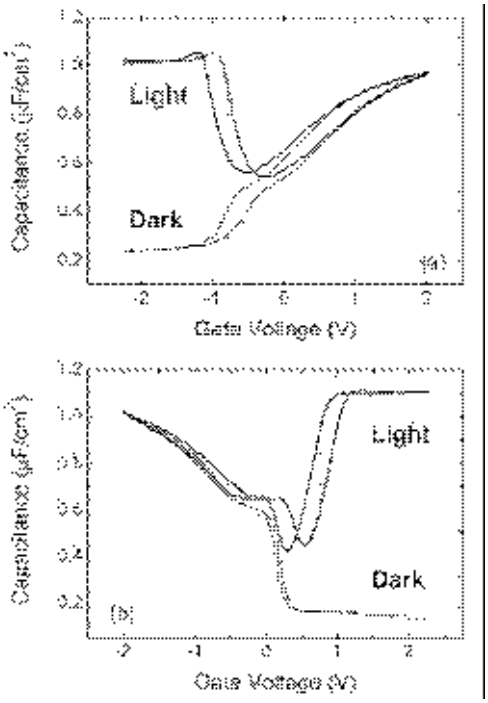


Fig. 3. C-V Characteristics in dark and under peripheral illumination for MOS capacitors with HfO_2 gate dielectrics and a-Si/SiO_2 interlayer on (a) n-type and (b) p-type GaAs

A self-aligned GaAs MOSFET with HfO_2 gate dielectrics was fabricated as shown in Fig. 4 [14]. A 10 nm thick HfO_2 dielectric was deposited by MOCVD at 400 ^oC on undoped GaAs substrates. The sample was then annealed at 600 ^oC and 50 nm of CVD-W was deposited. After the gate electrode patterning by drying etching, self-aligned source and drain regions were formed using Si^+ ion implantation. Deep p-well and shallow n-channel regions were then implanted through the W gate electrode, and the sample annealed at 900 ^oC for 5 seconds. Finally, contacts were formed by patterning and lifting off AuGeNi. Both enhancement- and depletion-mode devices were demonstrated as shown in Fig. 5. The threshold voltage was adjusted through the n-channel implant dose and energy.

In summary, carrier inversion in HfO_2-gated GaAs MOS capacitors with α-Si/SiO_2 has been demonstrated. In addition, we demonstrate the operation of all-implanted, self-aligned GaAs MOSFETs. These results are a major step forward in achieving the ultimate goal of self-aligned, surface-channel, inversion-mode, high performance GaAs MOSFETs.

INDIUM GALLIUM ARSENIDE BURIED-CHANNEL MOSFETS

As discussed in previous sections, surface-channel devices would require the formation of an extremely-high-quality semiconductor-dielectric interface in order to preserve low D_{it} near the surface-layer conduction-band edge. The buried-channel design is less sensitive to III-V/dielectric interface

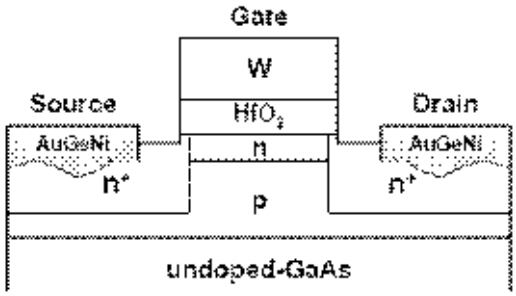


Fig 4. Schematic cross-sectional diagram of self-aligned GaAs MOSFET

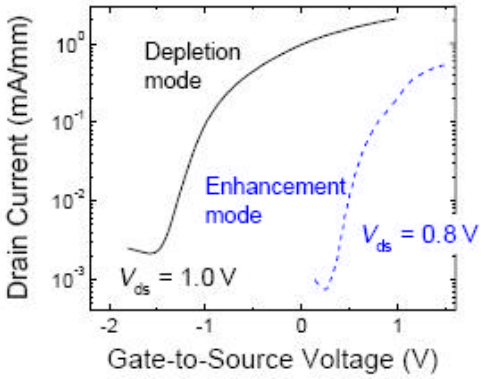
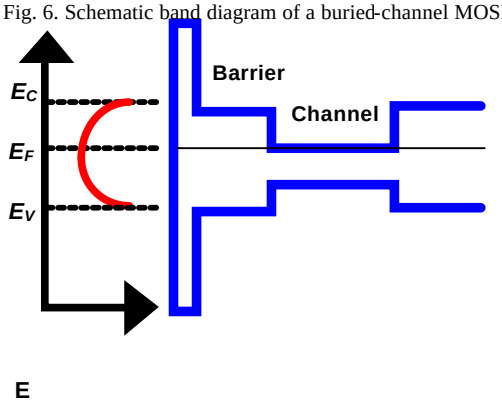


Fig. 5. I_d vs. V_{gs} plot of enhancement- and depletion-mode GaAs MOSFETs.

non-idealities because it allows the device to operate in a regime where the surface Fermi-level is far from the band edges of the surface semiconductor layer as shown in Fig. 6.

For buried-channel structures, the InGaAs/InAlAs material system is one of the most promising material systems for this application due to its large conduction-band offsets and high

Fig. 6. Schematic band diagram of a buried-channel MOSFET



carrier mobility. Schottky-gated InGaAs HEMTs grown on InP substrates have produced g_m values over 2 S/mm [11], and shown to compare favorably in terms of power-delay product [12] Despite these promising results, for ULSI logic

applications, InGaAs-channel FETs will ultimately need to incorporate high-① insulating gate dielectrics in order to meet ITRS leakage requirements.

In our previous work, we demonstrated the operation of $In_{0.7}Ga_{0.3}As$ buried-channel MOSFETs with HfO_2 gate dielectrics [15].However, the structure used in that work was not optimal due to its large surface-to-channel distance and δ-doping above the quantum well. In this paper, we demonstrate an enhancement-mode long-channel MOSFETs that utilize an undoped-buried-channel design and high-① dielectrics as shown in Fig. 7.

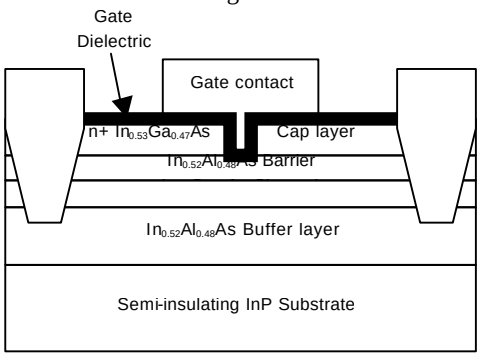


Fig. 7. The schematic cross-sectional diagram of an $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ undoped-buried-channel MOSFET.

The DC output characteristics of a typical buried $In_{0.7}Ga_{0.3}As$-channel MOSFET with L_g = 5 μm are shown in Fig. 8. The devices show good saturation and pinch off characteristics. The devices operate in enhancement mode and have a threshold voltage of 0.25 V, and drain current on-off ratio is ~10^4, A peak mobility of 1100 cm^2/Vs (after correction for external resistance) was determined at a carrier density of 2.6 x 10^{12} cm^{-2}. Further improvements should be possible through optimization of the interface properties.

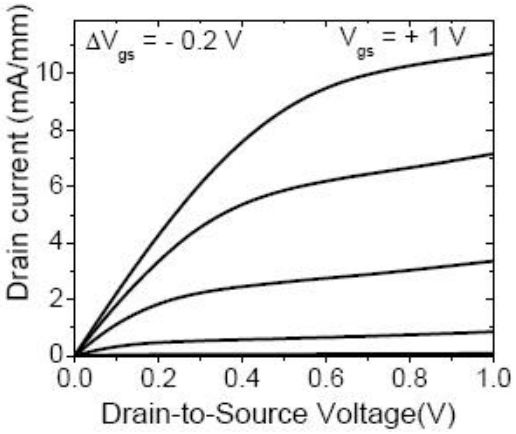


Fig. 8. Output characteristics of an enhancement-mode InGaAs buried-channel MOSFET with L_g = 5μm

The results of buried-channel MOSFETs are encouraging due to the fact that good modulation of the $In_{0.7}Ga_{0.3}As$ channel with positive threshold voltage has been achieved despite the fact that little optimization of the high-①/semiconductor interface was performed. The results support the hypothesis that the buried-channel design is less sensitive to III-V/ dielectric interface non-idealities because it allows the device to operate in a regime where the surface Fermi-level is far from the band edges of the surface semiconductor layer. Further EOT scaling is necessary to determine the degree to which high mobility can be maintained as the top barrier layer thickness is reduced, and ultimately find the optimum trade off between mobility and gate capacitance in these structures.

CONCLUSIONS

In conclusion, as the end of Si CMOS scaling is clearly in sight, III-V compound semiconductors have received renewed attention as the channel materials for future generation CMOS applications due to their high bulk electron mobility. However, in order to implement III-Vs in manufacturing CMOS technology, we have to overcome the challenges including an effective gate stack solution and integration with Si substrate and Ge pMOSFETs. In this paper, we demonstrate functional enhancement-mode GaAs-, and InGaAs- channel MOSFETs, with high-① gate dielectrics. These results are promising for realizing scalable III-V channel MOSFETs suitable for future VLSI logic applications.

ACKNOWLEDGEMENTS

The authors would like to thank Ghavam Shahidi for encouragement, support, and leadership, and Robert Sandstrom for fabrication support.

REFERENCES

[1] D. K. Sadana, ECS 210th Meeting, 2006, Oct 2006
[2] M. V. Fischetti, unpublished, 2001.
[3] S. E. Thompson, et al., IEEE Elect. Dev. Lett. 25, 191 (2004)
[4] K. Rim, et al., VLSI Technology. Dig. of Tech, papers, 59 (2001)
[5] S. Tiwari, et al., IEEE Elect. Dev. Lett. 9, 488 (1988).
[6] D. S. L. Mui, et al., Appl. Phys. Lett. 59, 2847 (1991)
[7] A. Callegari, et al., Appl. Phys. Lett. 85, 2540 (1991)
[8] M. Hong, et al., Jour. of Vac, Sci. & Tech. B 14, 2297 (1996)
[9] J. M. Woodall et al., Phys. Rev. Lett. 51, 1783 (1983)
[10] P. D. Ye, et al., IEEE Elect. Dev. Lett. 24, 209 (2003)
[11]D. Xu et al., IEEE Elec. Dev. Let. 20, 206 (1999)
[12]D.H. Kim et al., IEDM Tech. Dig., 787, (2005)
[13]S. J. Koester et al., APL 89, 042104 (2006)
[14]S. J. Koester et al., Device Research Conference, 43 (2006)
[15]Y. Sun et al, Device Research Conference, 49 (2006)