High-Performance BiHEMT HBT / E-D pHEMT Integration

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Abstract

We report on the status of TriQuint's BiHEMT process -- the cointegration of TriQuint's InGaP/GaAs HBT power amplifier technology with an InGaAs/AlGaAs E/D-Mode pHEMT technology into a single GaAs process. This added pHEMT functionality over previously reported GaAs HBT/FET cointegration technologies adds an additional level of versatility and potential circuit applications. Potential applications include the cointegration of HBT power amplifier circuitry with pHEMT-based bias control and logic circuitry, RF switches, and low noise amplifiers. The growth and process technologies developed for this process, as well as the preliminary device characteristics and process features, will be described. Finally, we will describe the process and performance tradeoffs featured in the BiHEMT process.

INTRODUCTION

The idea of cointegration of HBTs and FETs on GaAs has long been of wide interest [1-3] in the GaAs community. Of course, the principle attraction is in improving circuit functionality, analogous to Si BiCMOS technology. Recently, there has been a great deal of interest in combined HBT/FET processes for enhanced circuit functionality, particularly for power amplifier circuits. With a combined HBT/FET technology in GaAs, HBTs may be used for linear power amplification and FETs for logic and control circuitry, RF switches, and low noise power amplification. Two distinct approaches, each with their own advantages, have been described recently. One features manufacturability and simplicity of process at the expense of device performance by cointegrating a MESFET structure into the emitter of the HBT [4]. The other offers improved device performance by cointegrating a pHEMT epitaxial structure in the subcollector of the HBT [5], at the expense of additional processing steps and more complex crystal growth. However, in the latter approach the pHEMT epitaxy and process still represent a compromise between compatibility with the HBT epitaxial structure and device performance.

In the BiHEMT approach reported here, the design goals are somewhat different from those reported previously [4,5], with a goal of maximizing pHEMT functionality and device performance (while maintaining minimal impact on HBT performance) for improved circuit functionality. The result is a novel epitaxial design and process architecture that replicate as closely as possible TriQuint's existing HBT and E/D pHEMT processes.

EPITAXIAL LAYER DESIGN AND GROWTH

The epitaxial structure is relatively straightforward. Aside from several minor modifications that are driven by process considerations, the BiHEMT epitaxial structure consists of the TriQuint HBT epitaxial structure on top of the TriQuint E/D pHEMT epitaxial structure.

In order to minimize BiHEMT cost, a single MOCVD growth is used for the entire epitaxial structure, without the need for regrowth or intermediate processing. The requirement of high pHEMT performance necessitates placement of the entire InGaAs/AlGaAs pHEMT epitaxial stack underneath the HBT subcollector. In other words, there is no part of the HBT subcollector proper that is used in the active pHEMT device, unlike the case reported in [5]. That way, not only is the pHEMT well isolated from parasitic capacitances, but no compromises in epitaxial structure are made that might lead to significantly degraded performance. Naturally, special care needs to be taken to ensure minimal degradation in pHEMT characteristics during the long subsequent HBT growth. A key requirement of a high-performance pHEMT device is high maximum current I_{max} and minimal on-resistance R_{on}; some small modifications in the pHEMT epitaxial structure must be made in order to minimize pHEMT epitaxy degradation during the subsequent HBT growth. Maintaining the I_{max} and R_{on} of the original E/D pHEMT process in the BiHEMT process is challenging.

Of course the pHEMT epitaxy technically forms a part of the subcollector of the HBT, since it is a conductive region immediately underneath the subcollector. Nonetheless, the sheet conductivity of the pHEMT structure is negligible in comparison to that of the subcollector, as the pHEMT active layers are relatively thin compared to the subcollector. Since precision is required in etching to the appropriate pHEMT epilayer, etch stop layers are required for process ease at several points in the epitaxy. These layers are intentionally kept thin to avoid process complexity. Their effect on HBT thermal resistance is minimal, since they are underneath the active HBT epitaxial layers and where the HBT

structure is physically widest. Additionally, a large part of HBT self-heating is dissipated through a thermal shunt on top of the active emitter.

DEVICE FABRICATION

The BiHEMT process represents a modification of TriQuint's HBT process, with pHEMT specific steps inserted between the HBT device-specific process steps and the passive/interconnects metallization formation.

Fig. 1 shows a cross-sectional schematic of TriQuint's HBT and E/D pHEMT technology. Device fabrication is relatively straightforward, with four types of process steps: HBT-specific metallization, such as at emitter and base; etches that uncover the different HBT and pHEMT epi layers; pHEMT-gate processing; and the fabrication of common structures, such as capacitors, resistors, and metal interconnects. In order to reduce process complexity, several device-specific process steps, such as HBT collector and pHEMT source/drain ohmic metallization are combined. No degradation is seen in either pHEMT or HBT device characteristics as a result of this consolidation. Fabrication starts with standard HBT processing modules, including emitter metallization, emitter mesa formation, and base metallization.

Then, the base mesa is formed by etching all the way down to an etch stop at the top of the subcollector. Once the subcollector is reached, an additional etch step is added that etches away the subcollector in the field, in order to uncover the pHEMT epitaxial structure. pHEMT processing then begins with wide recess pattern lithography and etch, and a shallow implant is performed into the remaining pHEMT epi in the field in order to electrically isolate all devices.

After the implant, a common HBT/pHEMT ohmic metallization is done, with the collector metallization sitting on top of the subcollector for the HBT and lower down in the epi, on top of the cap layer, for the pHEMTs. Following ohmic contact formation comes the proprietary D-mode and E-mode narrow recess formations and gate depositions; for both types of device, etch stops facilitate the recess and 0.7 um gates are formed. Here we note that our usual E/D process employs a 0.5 um gate. A 0.5 um gate BiHEMT process is currently under development, but narrow gate lithography is considerably complicated by the highly nonplanar BiHEMT structure.

After HBT and pHEMT device formation, 50 ohm/square NiCr resistors are formed, as well as MIM capacitors with 1200 pF/mm^2 capacitance. The bottom of the MIM layer is used as a local interconnect, and subsequent plated gold layers of 2 um and 4 um thickness are used for global interconnects. Finally, the entire

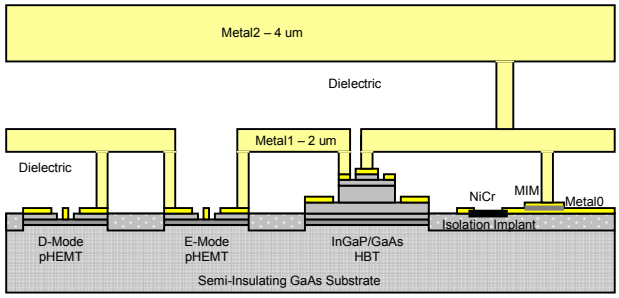

Figure 1. Cross section of TriQuint's BiHEMT process, showing GaAs/InGaP HBT, D-mode AlGaAs/InGaAs pHEMT, E-mode AlGaAs/InGaAs pHEMT, resistors, capacitors, and three levels of interconnect metal.

structure is covered by a thick layer of nitride for passivation, and wafer thinning and through via formation follow.

BiHEMT DEVICE CHARACTERIZATION

As previously mentioned, HBT-specific epitaxy and process in the BiHEMT process are for the most part unchanged from the standard HBT process. As a result, most HBT device parameters – both DC and RF – are substantially the same as they are in the original TriQuint HBT power amplifier process. Fig. 2(a) and (b) shows representative Gummel plot and common-emitter I-V characteristics for a 3x(3x45) um^2 emitter HBT. Typical beta is 80 and BV_{cbo} = 24 V, with F_t = 30 GHz and F_{max} = 55 GHz.

There are only two significant differences in HBT characteristics between the BiHEMT HBT and our dedicated HBT process. First, the BiHEMT HBT has a slightly higher collector resistance. This is because in the

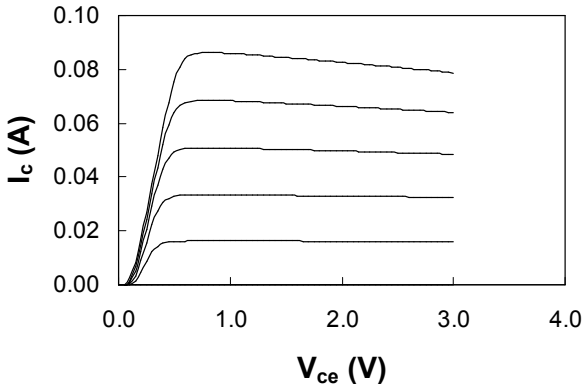

Fig. 2(a). Common-emitter I-V for a 3x(3x45) um^2 emitter HBT in the BiHEMT process.

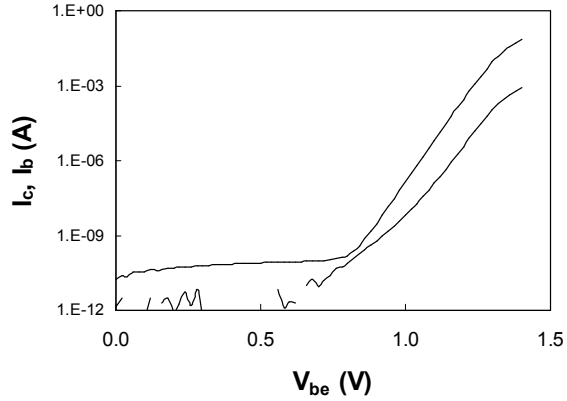

Fig. 2(b). Gummel plot for the HBT in Fig. 2(a).

BiHEMT process, the subcollector is grown thinner in order to reduce nonplanarity, as this layer has to be etched completely off in the field. Second -- and related to this -- isolation and leakage current between HBT structures is lower in the BiHEMT process, because the remaining epitaxy in the field is thinner and can be isolated with a shallower, lower dose isolation implant than is the case with the HBT process.

As expected, BiHEMT FET performance is similar to that of our nominal E/D pHEMT process performance, but with some change seen due to the 0.7 um gates in the BiHEMT. Fig. 3(a) shows the DC I-V characteristics of a typical D-mode device with a 0.7 um gate and 150 um gate width. Fig. 3(b) shows the transfer characteristics. As shown, peak g_m is 300 mS/mm, Idss is 160 mA/mm, and I_{max} is 420 mA/mm. Pinchoff voltage V_p is -0.8 V, gate-drain breakdown voltage BV_{gdo} is 22 V, and on resistance R_{on} is 2.0 ohm-mm. RF characteristics include a typical F_t of 20 GHz and an F_{max} of 57 GHz.

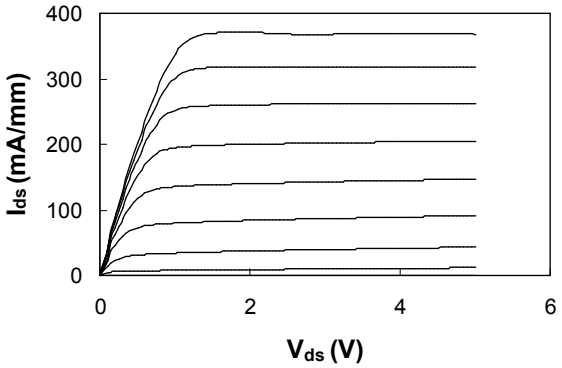

Fig. 3(a). DC I-V characteristics of a D-Mode pHEMT with 0.7 um gate length and 150 um gate width. Vg = -0.8 to 0.8 V, in 0.2 V steps.

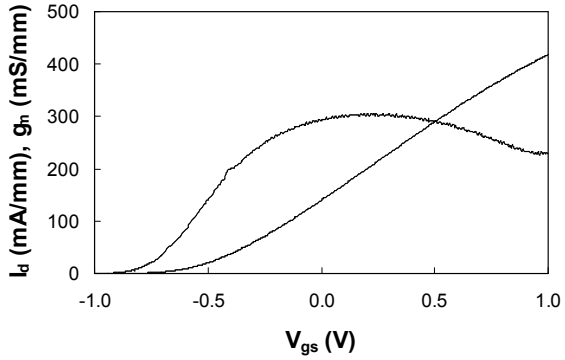

Fig. 3(b). Transfer curves for the D-mode pHEMT in Fig. 3(a) for V_d = 2 V.

DC I-V characteristics of a typical E-mode BiHEMT device are shown in Fig. 4(a) for a device with a 0.7 um gate length and 150 um gate width. Fig. 4(b) shows the transfer characteristics. As shown, peak g_m is 460 mS/mm and I_{max} is 240 mA/mm. Pinchoff voltage V_p is +0.3 V,

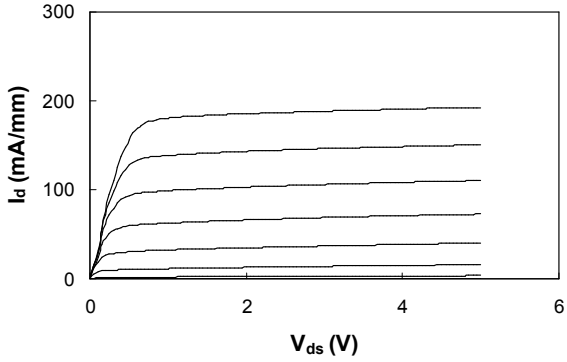

Fig. 4(a). DC I-V characteristics of a E-Mode pHEMT with 0.7 um gate length and 150 um gate width. Vg = 0.2 to 0.8 V, in 0.1 V steps.

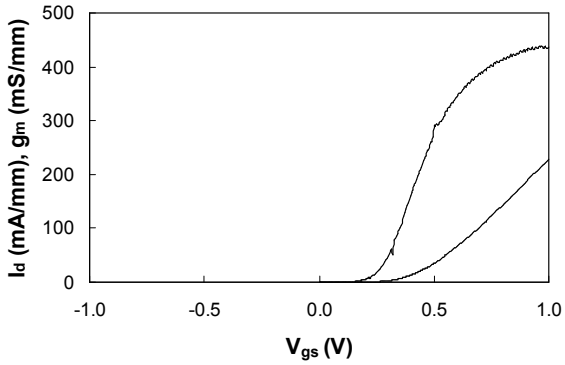

Fig. 4(b). Transfer curves for the E-mode pHEMT in Fig. 3(a) for V_d = 2 V.

gate-drain breakdown voltage BV_{gdo} is 23 V, and on resistance R_{on} is 2.3 ohm-mm. RF characteristics include a typical F_t of 22 GHz and an F_{max} of 65 GHz. Future work will focus on improving pHEMT performance (focusing on the development of a 0.5 um gate process) and ramping the BiHEMT process to volume production.

SUMMARY

We have described TriQuint's BiHEMT process. Applications for this technology include the cointegration of HBT power amplifiers with E/D pHEMT-based logic and control circuitry, RF switches, and low noise power amplifiers. This process features three levels of metal, 50 ohm/square resistors, and 1200 pF/mm^2 MIM capacitors. The epitaxial structure is a unique combination of our existing HBT and E/D pHEMT epitaxy, and fabrication is optimized to deliver the highest level of transistor performance possible. The HBTs exhibit nearly identical performance to our existing HBT power amplifier process; the E/D pHEMTs feature 0.7 um gates with good RF performance, high current density, and low on-resistances.

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REFERENCES

1. D.L. Plumton, et al., "Method to Integrate HBTs and FETs", U.S. Patent No. 5,077,231 (1989).
2. D. Cheskis, et al., IEDM Tech. Digest, pp. 91-94 (1992).
3. D. Streit, et al., GaAs IC Symp. Tech. Digest, pp. 329-332 (1994).
4. M. Sun et al., Proc. CS MANTECH Conf., pp. 149-152 (2006).
5. M. Shokrani et al., Proc. CS MANTECH Conf., pp. 153-156 (2006).