Monolithic Integration of E/D-mode pHEMT and InGaP HBT Technology on 150-mm GaAs Wafers

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Abstract

Wafer-level integration of GaAs enhancement-mode pHEMT, depletion-mode pHEMT and HBT (H2W is the code name at WIN) is a very appealing technology, which offers a number of significant advantages over conventional device technologies. In this paper, we report the development status of the H2W at WIN Semiconductors. MOCVD-grown epitaxial material is selected with InGaP HBT on top of pHEMT device to minimize the potential drawback of excessive parasitic compared to the pHEMT atop of HBT structure. Critical process steps, such as gate photolithography and gate recess process control, will be discussed and presented. The ED-pHEMT and HBT electrical performance (DC, small signal, noise, and power) and uniformity data will be included in the paper as well. Functional building blocks, such as high power switches and power amplifiers, based on the H2W technology will also be demonstrated

INTRODUCTION

Wafer-level integration of GaAs HBT and E/D-mode pHEMT (H2W is the code name of this integration technology at WIN) can make a significant impact on the design of RF transceiver integrated circuits [1]-[3]. The H2W technology offers great design flexibility and novel circuit opportunities by combining the advantages of HBT's high current driving ability, excellent output power density, and low 1/f noise, as well as pHEMT's low RF-noise, low threshold voltage and lower power consumption. Therefore, the monolithic integration of logic control circuits, RF-switches, low noise amplifiers, and power amplifiers can be realized in a single GaAs chip. From foundry's point of view, we should provide high integrated process and multi-functional devices for RF-IC designers to satisfy the endless demand of compact die size with low manufacturing cost for commercial mobile market.

In this paper, we report the development status of WIN H2W technology, which includes the design of epitaxial structure, process flow and critical gate photolithography. In addition to devices fabrication, after evaluating the device-level dc, small-signal, rf performance, we demonstrated the InGaP HBT power amplifier, D-mode pHEMT single-pole double-through (SPDT) power switch, and elementary E/D-mode pHEMTs logic gates with the H2W technology.

EPITAXIAL STRUCTURE DESIGN

Fig. 1 shows the schematic H2W epitaxial structure, which is grown by the MOCVD on 150-mm semi-insulating GaAs substrate. A stacked layer structure with InGaP HBT on top of pHEMT was designed with the following advantages: (1) It is suitable for high volume with low manufacturing cost as compared with the selective re-growth technique [2]; (2) It avoids the MOCVD growth temperature restriction (normally, the pHEMT growth temperature is higher than HBT for performance and reliability consideration), and eliminates the generation of additional parasitic capacitance in the pHEMT device; (3) Furthermore, the InGaP etch-stop layer was used to fully separate the HBT and pHEMT, and there is no HBT and pHEMT shared layer in the designed structure, which is able to separately optimize the HBT and E/D-mode pHEMT performance without trading off with each other.

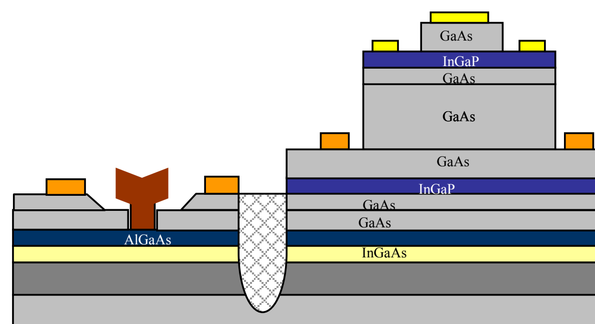

Fig. 1 The schematic epitaxial structure cross-section of the H2W technology.

The HBT structure was designed to provide excellent power performance with high ruggedness characteristics for wireless mobile applications. As to the pHEMT, the epitaxial structure was designed to be compatible with double selective gate recess etch process using AlGaAs and InGaAs as the Schottky layer and channel layer, respectively. The layer thickness, doping concentration, and group III element mole fraction was designed to obtain the optimum trade-off among parameters, such as breakdown voltage, on-resistance, pinch off voltage, transconductance, and gate lag.

PROCESS FLOW

The fabrication process starts from HBT emitter mesa etch followed by base metal formation, base mesa etch, and collector mesa etch. Then the ohmic contacts were formed by electron beam evaporation for collector contact of HBT and source/drain contacts of pHEMT's. Device isolation is done by ion implantation followed by the selective first recess etch. Due to the high topology feature of HBT, obtaining uniform 0.5-μm single and multiple-gate pHEMT devices across a 150-mm wafer is the greatest process challenge in H2W technology development. The gate metals, Ti/Pt/Au and Pt/Ti/Pt/Au, were deposited for D-mode and E-mode pHEMT, respectively. Fig. 2 shows the SEM cross-section of single and trip-gate devices. It is shown that WIN H2W technology exhibits multiple-gate process ability, which can be used for high isolation and high linearity switch application.

After the gate metallization, the HBT and pHEMT were fully passivated by SiN, and followed by TaN resistor with sheet resistance 50 ohms/square. Two interconnection metal levels and 100 nm SiN were used for 600 pF/mm2 MIM capacitor. Polymide bridge and protect nitride were adopted for reliability concern. After front-side process completed, substrate is thinned down to 75-μm and through-via holes are formed by ICP etch. A 4-μm thick Au film is plated as the backside metallization. Fig. 3 shows the cross-sectional SEM photographs of a fully completed H2W HBT and pHEMT separated by 25 μm.

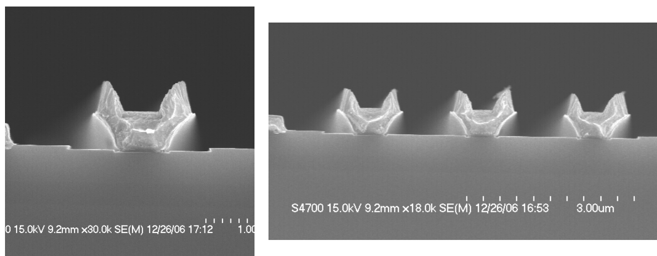

Fig. 2 SEM photographs of single- and triple- gate formed by using bi-layer photo-resist process in H2W technology.

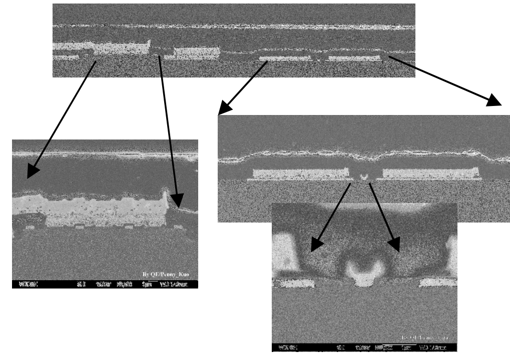

Fig. 3 Cross-sectional SEM's of the HBT and pHEMT devices from a 150-mm GaAs wafer.

E/D-MODE PHEMT DEVICE CHARACTERISTICS

The E/D-mode pHEMT dc transfer characteristics are shown in Fig. 4, which exhibits excellent device pinch-off characteristics. The threshold voltage (I_{ds}=1mA/mm) and the I_{dss} are -0.8 V and 150 mA/mm for the D-mode pHEMT and +0.35 V and 0.02 μA/mm for the E-mode pHEMTs, respectively. On-wafer microwave S-parameter evaluation was carried out by using network analyzer. The values of f_T extracted at biases of V_{ds}= 3 V and V_{gs} was chosen for maximum transconductance are 22 GHz and 25 GHz for the D-mode pHEMTs and the E-mode pHEMTs, respectively. The corresponding f_{max} values are 83 GHz and 99 GHz. Table 1 summarizes the relative characteristics of E/D-mode pHEMT's.

Table 1 Summary of DC and RF characteristics of ED-mode pHEMT's.

D-mode pHEMT						
V_{to} (volt.)	I_{dss} (mA/mm)	V_{dg} (Volt.)	g_m (mS/mm)	R_{on} (ohm.mm)	f_t (GHz)	f_{max} (GHz)
-0.8	150	20	270	2.5	22	83
E-mode pHEMT						
V_{to} (volt.)	I_{dss} (mA/mm)	V_{dg} (Volt.)	g_m (mS/mm)	R_{on} (ohm.mm)	f_t (GHz)	f_{max} (GHz)
+0.35	0.02	20	400	3.3	25	99

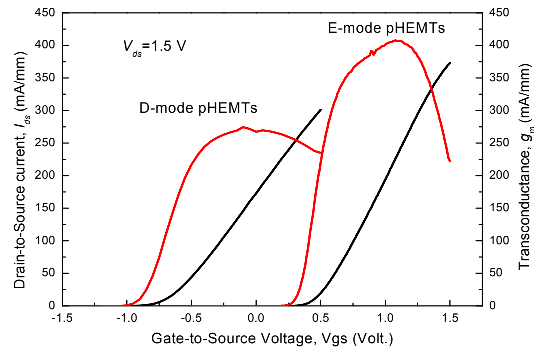

Fig. 4 DC I_{ds}-g_m-V_{gs} characteristics of the AlGaAs/InGaAs pHEMT's in the H2W technology.

Fig. 5(a) shows the output power and power-added efficiency (PAE) versus input power of a 4 × 75 µm E-mode pHEMT biased at V_{ds} = 5 V, I_{ds}=130 mA/mm. The maximum PAE of 46% with output power of 452 mW/mm was obtained at 3.5 GHz. Regarding the noise performance, the 8 × 25 µm E-mode pHEMT exhibits 0.5 dB minimum noise figure at 3 GHz with 16 dB associated gain biased at V_{ds}= 3 V and I_{ds}= 60 mA/mm, as shown in Fig. 5 (b).

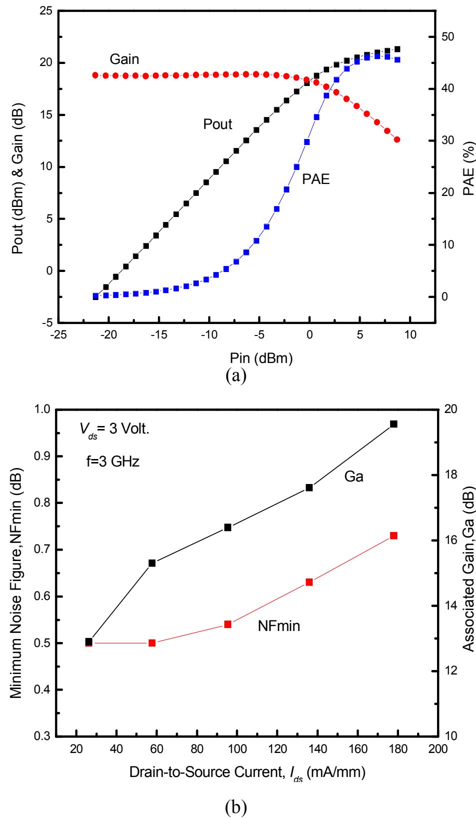

Fig. 5 RF power (a) and noise performance (b) of E-mode pHEMT's.

SPDT HIGH POWER SWITCHES

Fig. 6 shows the schematic circuit topology of a single-pole-double-throw (SPDT) switch for evaluation of H2W technology multi-gate process. The switch demonstrates the insertion loss (Tx-Ant) of 0.48 dB and isolation greater than (Tx-to-Rx) 20 dB at 900 MHz. To further investigate the linearity characteristics of SPDT switch, the harmonic testing was carried out, and the results are shown in Fig. 7. In the Ant-port, an 70 dBc second-harmonic rejection ratio and an 75 dBc third-harmonic rejection ratio were measured at Tx-to-Ant input power of 35 dBm, where the control voltages are –2.5 V and 0 V for Rx and Tx, respectively, as shown in Fig. 7. It clearly shows that the H2W optical gate lithography process is suitable for multiple gate high power and high linearity applications under low control voltage.

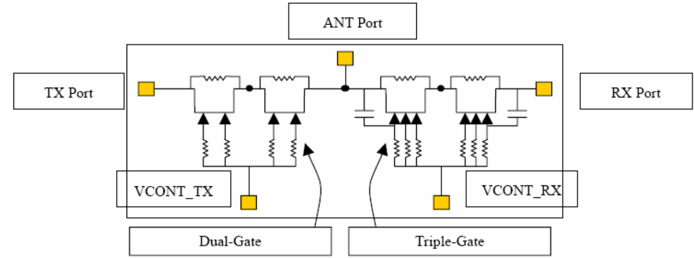

Fig. 6 The circuit schematic of a high power SPDT switch.

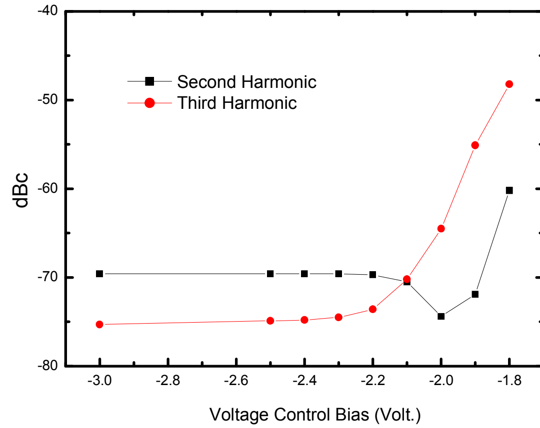

Fig. 7 the second and third harmonic reject ration measurement results of a SPDT switch.

LOGIC GATES

Due to no offset voltage and low knee voltage in pHEMT devices, logic gates by using E/D-mode pHEMTs are the important components for RF systems such as multi-mode bias control. Fig. 8 demonstrates an inverter and a NAND as elementary logic gates using the H2W process. The power consumption is only 0.88 and 0.33 mW for inverter and NAND gates, respectively, by using device size ratio of 1:2 (10-µm for D-mode pHEMT, and 20-µm for E-mode pHEMT).

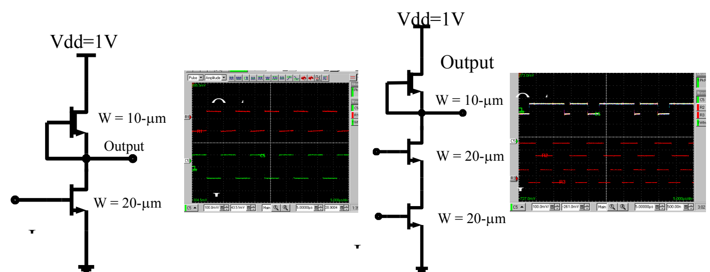

Fig. 8 The circuit schematic of elementary logic gates by using E/D-mode pHEMT.

HBT and Power Amplifier Characteristics

The typical turn-on voltage for the InGaP HBT is 1.26 V. The base layer is designed with dc current gain of 75. Table 2 summarizes the critical DC and RF parameters of the developed H2W HBT.

Table 2 Summary of DC and RF characteristics of InGaP HBT in H2W process

InGaP HBT						
BV_{cbo} (volt.)	BV_{ebo} (Volt.)	BV_{eco} (Volt.)	β	$V_{turn\text{-}on}$ (Volt)	f_t (GHz)	f_{max} (GHz)
31	7	20	75	1.26	31	110

Fig. 9 shows the IV curve of a discreet power chip mounted on a FR4 evaluation board with 11520-µm^2 total emitter area. To further evaluate the power performance, the input and output matching networks were tuned for maximum linear gain. The output power and power-added efficiency (PAE) versus input power are shown in Fig. 10 with V_{ce} = 3.6 V and I_{ce}= 200 mA by fixing the V_{be}. The power amplifier is able to deliver approximately 34.5dBm output power with a peak power-added efficiency (PAE) of 63%.

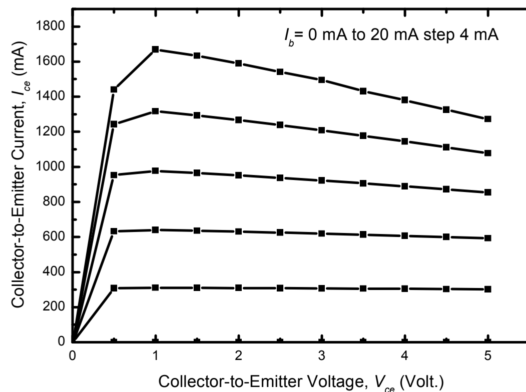

Fig. 9 IV curves of a 11522-µm^2 HBT power device.

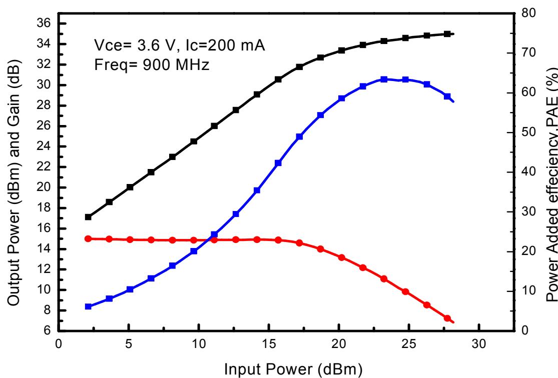

Fig. 10 Measured output power, gain, and PAE versus input power characteristics of HBT power amplifier.

As shown in Fig. 11, the device can withstand significant high current stress under output impedance mismatch (VSWR=12:1 for all phases) at Vce = 3.6 V and input power = 27 dBm. This demonstrates that the HBT of H2W technology possesses high roughness characteristics without sacrificing power performances.

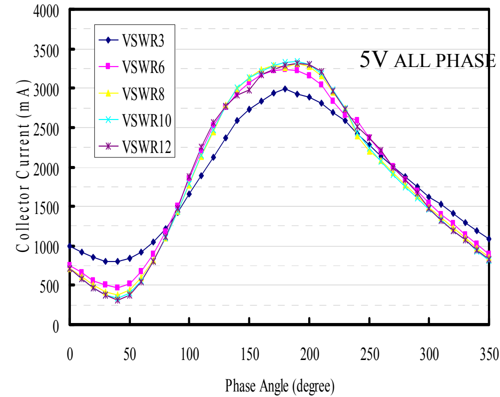

Fig. 11 The collector current of HBT power device versus various phase angles under different output matching conditions.

Summary

In this paper, we summarize the fabrication and characteristics of the H2W technology. MOCVD-grown epitaxial material is selected with InGaP HBT on top of pHEMT device to minimize the potential drawback of excessive parasitic compared to the pHEMT atop of HBT structure. The challenge of forming 0.5-µm multiple gate fingers on high topology wafer with controllable small un-gated region was overcome using double selective recess process combined with dual-layer gate photolithography process to offer sufficient breakdown voltage and to minimize the surface charge effect for both E- and D-mode pHEMT's. The ED-pHEMT and HBT electrical performance (DC, small signal, noise, and power) are presented. Functional building blocks, such as high power switches and power amplifiers, based on the H2W technology are also demonstrated with satisfactory performance. The results represent this technology offers a great potential and degrees of freedom for design of power amplifiers, high-integrated RF transceivers and opportunity for novel RFIC circuits.

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