Development and Ramping of pHEMT in an "HBT Fab"

Mike Fresina, C. Barratt, C. Duncan, S. Greene, W. Lewis, L. Li, T. Rogers,
C. Santana, W. Wohlmuth, and R. Yanka

RFMD, 7628 Thorndike Road, Greensboro, NC 27403, www.rfmd.com, mfresina@rfmd.com

KEY WORDS: *HBT, pHEMT, integration, manufacturing*

INTRODUCTION

In the last 10 years RFMD has gone from a fabless RF integrated circuit company to having the largest GaAs wafer manufacturing capacity in the industry. This success has been aided by the singular focus of producing only HBT wafers for cellular power amplifiers. However, to support increasing integration requirements, specifically those of front-end and TX modules, we have recently added a pHEMT process for switches. In this paper we will discuss the challenges, opportunities and lessons learned in developing and ramping a pHEMT process in what had been up to that point an HBT fab.

The first wafer fab at RFMD (Fab-1) was shipping 4-inch AlGaAs/GaAs HBT wafers by 1998. The first half of the second GaAs fab (Fab-3) was a copy of Fab-1 (still 4-inch) and was in production by 2002. In 2003 we completed a 6-inch conversion of the first half of Fab-3 and in 2006 completed an expansion into the second half of Fab-3. Until recently, all of this capacity was supporting production of 5 different generations of AlGaAs and InGaP HBT processes. However, in 2003 we began development of a pHEMT process which was production released in early 2005 with significant volume ramping in 2006.

PROCESS DEVELOPMENT

When developing any new technology the ability to re-use processes and operations not only expedites the development cycle but also increases the likelihood of success in manufacturing. This was a primary consideration in developing a pHEMT process at RFMD. As is illustrated in Figure 1, we reused HBT ohmic contact, emitter metal (for the gate) and implant for the pHEMT active device and silicon nitride and interconnect metal for the backend.

In several cases we were not able to reuse operations as-is but only had to make minor changes (for example to a clean in a photo operation). But these modifications were made only after technical gaps were confirmed and tradeoffs were evaluated. This helped maintain tool flexibility and minimize new failure modes due to tool, process and workforce execution.

New process development was required for the gate – channel features but even there we were able to use an existing metal recipe for the gate. A bi-layer gate photo process was developed that allowed for independent control of gate length and the self-aligned, selective channel etch.

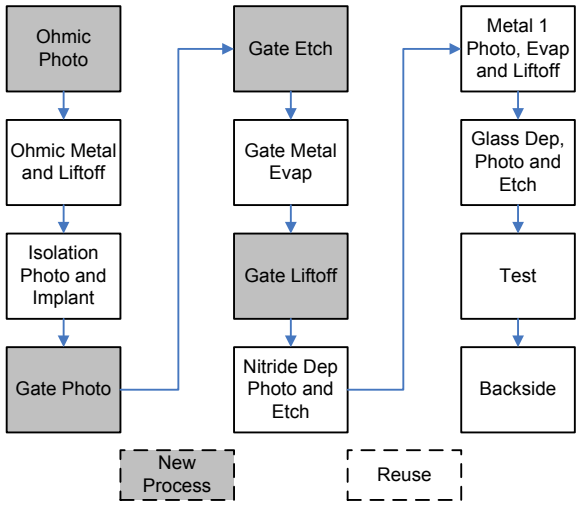

Figure 1. pHEMT process flow highlighting new versus reused process modules.

A Process FMEA was used to highlight sources of potential device variability and yield loss. Variation due to processing delays introduced by current work center layouts led to the relocation of certain systems within the fab work centers. This ensured more consistent surface condition of the channel immediately prior to the gate evaporation – a consideration unique to pHEMT and not a factor for any of our HBT metal processes.

INTEGRATION

To coexist with HBT production the pHEMT process had to be engineered to fit in the same fab environment by blending the differences between the HBT and pHEMT processes while maximizing the amount of reuse. Wafer fabs are job shops consisting of work centers that provide the process technologies necessary to produce the desired products (see Figure 2).

The work centers necessary for HBT fabrication are very similar to those necessary for pHEMT fabrication. Every required step in the HBT process is assigned to a work center such as photolithography, metallization, etch, test etc. To integrate a pHEMT process into an HBT fab it is necessary to assign the required steps to work centers and where particular work center capability does not exist it must be created. This would be done through the acquisition of assets, development of specific processes, work force training, process control protocols, new metrology and/or any other modification of a work center necessary to perform and control the new fabrication step. Through the emphasis on re-use we were able to minimize the amount of new capability required to be introduced but where necessary, prudent choices had to be made to insure the technical capability meshes with the needs of the fab.

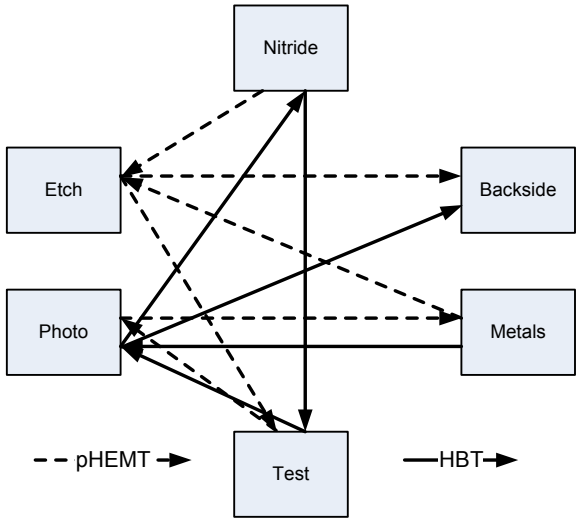

Figure 2. Illustration showing two different technologies (pHEMT and HBT) utilizing the same wafer fab "job shop."

Figure 2 depicts schematically how the work center routings might differ between HBT and pHEMT but can be managed in a factory setting where each work center is capable of supporting the necessary process technologies.

A specific example of a major difference was in the selective gate recess etch step. This was a new technology not used in HBT and its work center location was driven by the compromise between factory dynamic and technology requirement. Traditionally our etch processes were assigned to the etch work center. This allows the etch assets, metrology and expertise to be co-located since these are common for wet etch steps. However, we decided that the gate recess etch should be located in the metallization work center since the queue time between that operation and the gate metal deposition needed to be minimized. This meant adding the etch capability to the metallization work center along side the existing capabilities.

An example of a new operation developed from existing assets is monitoring the width of the pHEMT channel. The metrology systems eventually used for this

step were already being used to monitor critical HBT dimensions and were re-employed for use in pHEMT CD control. New parameters were introduced along with remedial action plans for dealing with out-of-control measurements in order to insure stability in pHEMT channel critical dimensions.

In this way HBT and pHEMT lots can coexists, move smoothly among work centers and appear in each work center as simply another lot to process. Optimizing the industrial engineering decisions that affect the Fab as well as the technical performance of the process are critical to the commercial success of the final outcome.

MANUFACTURING

As with any new process, not all of the challenge is in the development phase – additional issues will be discovered when releasing a process to production and there are the inevitable problems that only show up when running volume. Certain strategies were employed when developing and ramping the pHEMT process to educate the workforce and minimize the opportunity for mistakes.

During development several front-line operators assisted engineering by running tests and gathering data which gave them an early exposure to the new processes. The entire workforce required detailed training in these new processes once they were finalized and prior to production ramps. Some specific challenges in a few areas:

Photolithography. Added new photo-resists, coat/bake and develop programs, and the inspection of pHEMT-specific levels for new types of defects and problems. In particular, the gate-channel features were significantly smaller and visually different than seen on HBT technologies.

Metals. Introduced new timing and WIP flow limits on staging wafers prior to deposition, new etch chemistries, measurement techniques, metal liftoff chemistries and inspection techniques.

Test. On-wafer switch KGD required new test kits, probe cards, test set-up techniques, and responses to fails or questionable data. This was a particular challenge as there was a good amount of test development and refinement on-going while the process was being ramped.

Finally, pHEMTs posed a learning curve for both the workforce and for fab supervision as they learned how to manage WIP with pHEMTs running alongside older technologies. Issues such as having two technologies get the same metal deposition recipe but different liftoff recipes made staging at those points challenging as lots were batched and then separated at new points. Also, higher volumes of pHEMT pressured certain tool sets (such as implanters and evaporators) much more heavily than in the past, posing both capacity constraint concerns, skills or training issues, and difficulties with WIP management. With careful planning and with the support of process and test engineering at all phases of pHEMT ramping the manufacturing group was able to successfully handle these changes.

MBE METROLOGY

The development of RFMD's MBE growth process for pHEMT material drew extensively from our experience with high volume HBT production. Given the common material system, existing setup and characterization procedures were directly applicable to pHEMT production. Surface morphology, thickness, composition and electrical properties can all be controlled with a common characterization toolset. The use of accelerated processing of production samples to provide timely device performance feedback has been standard practice in HBT production. A similar procedure has also been implemented for

pHEMT. Differences do arise in the analysis required to extract the parameters of interest for the process being controlled. The goal remains the same, however: To provide high-throughput, non-destructive characterization of production material that can be directly correlated with device DCPCM data.

Structural and electrical characterization is carried out using x-ray diffraction, non-contact resistance measurements and Van der Pauw Hall analysis. In x-ray analysis of HBT's, simple peak separation calculations can be used to control composition in indium containing contact layers. A more sophisticated analysis of diffraction data from pHEMT structures provides overall growth rate, AlGaAs composition, InGaAs composition and channel thickness. Data collection and analysis is carried out on a commercial DCRC system with robotic wafer handling, allowing us to take measurements from every growth run.

Non-contact sheet resistance measurements are used for both HBTs and pHEMTs to monitor the electrical properties of the epi stack. Throughput is high enough that every wafer can be monitored. However, this technique does not separate the effects of individual conducting layers. It can only provide an overall sheet resistance. In pHEMTs, conduction takes place in the cap layer as well as the channel layer. Van der Pauw Hall measurements can be used to probe the characteristics of the channel layer. However, this typically requires destruction of a product wafer or the growth of "thin cap" structures to remove the effect of the cap layer.

In order to overcome the shortcomings of conventional Hall analysis of pHEMT structures, multi-field Hall measurements are used to screen production material at RFMD. Using a commercially available system, Hall measurements are carried out over a range of magnetic fields. Analysis of the combined data separates the effect of carriers in the cap and channel layers.

When applied to pHEMT structures, the technique provides sheet density and mobility values for the cap and channel layers. Measurements are made at room temperature on whole four or six inch production wafers. As implemented at RFMD, multi-field Hall measurements are non-destructive. No production material is lost and no production time is spent growing special Hall structures. Although throughput is somewhat lower than other characterization techniques, the information obtained is extremely valuable for predicting DC device performance.

CONCLUSIONS

Releasing a new technology into a mature facility requires careful planning and consideration to avoid compromising the new process or adversely affecting the incumbent capability. The more everyone (development engineering, manufacturing, internal customers) understands the issues and trade-offs in key decisions, the higher the probability of success.

ACKNOWLEDGEMENTS

The authors would like to thank the many engineers, technicians and operators without whose help this work would not be possible.

ACRONYMS

CD: Critical Dimension
DCPCM: Process Control Monitor (dc test)
DCRC: Double Crystal Rocking Curve
FMEA: Failure Mode Effects Analysis
HBT: Heterojunction Bipolar Transistor
KGD: Known-Good Die
MBE: Molecular Beam Epitaxy
pHEMT: Pseudomorphic High-Electron Mobility Transistor
TX: Transmit
WIP: Work In Progress